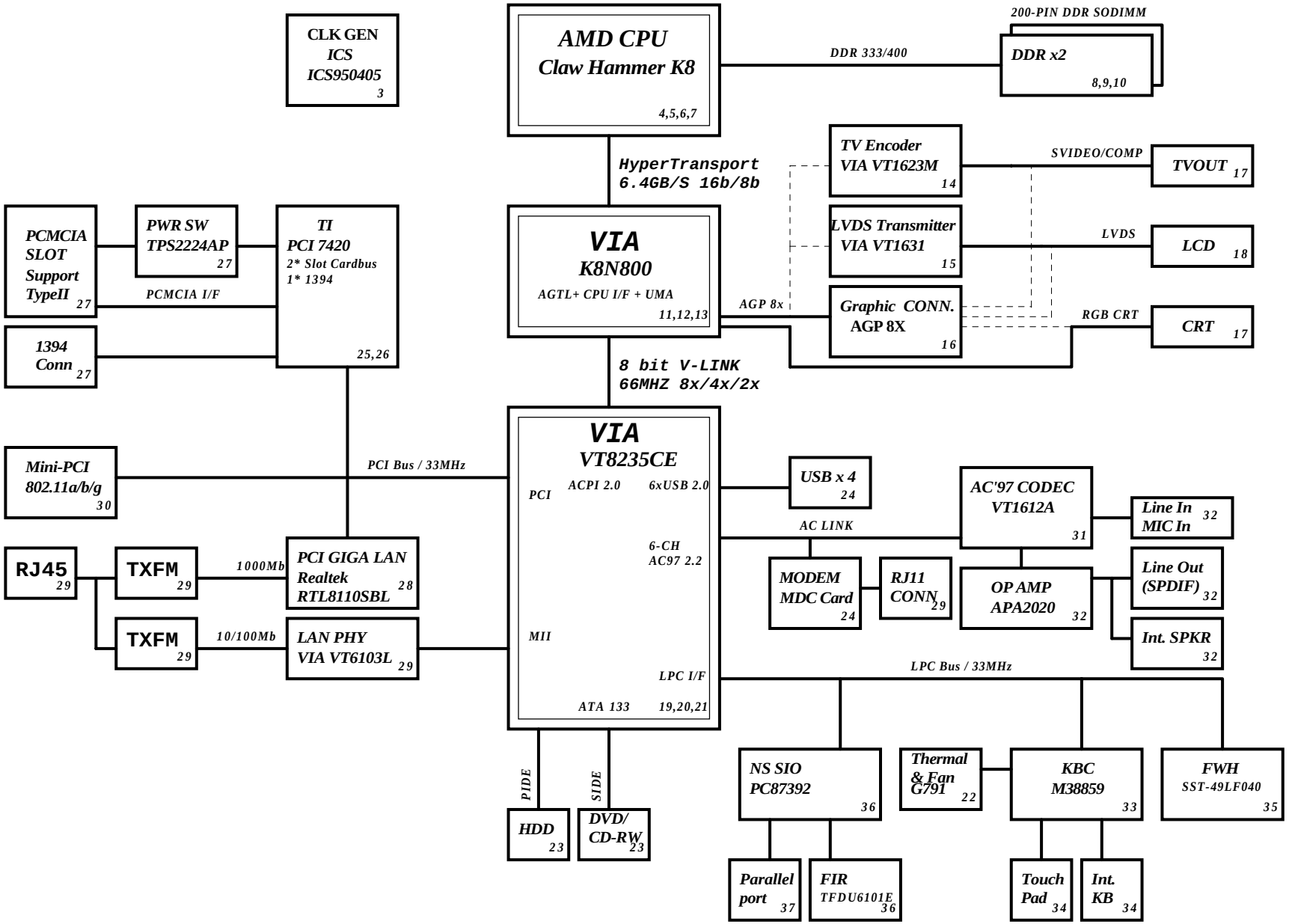
EGRET Block Diagram



PCB Layer Stackup
L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4

Battery Charger 46
MAX1645BEEI

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

SYSTEM DC/DC 43
MAX1999

INPUT	OUTPUT
DCBATOUT	5V_S5, 3D3V_S5

SYSTEM DC/DC 44
TPS5110

INPUT	OUTPUT
DCBATOUT 2D5V_S3	2D5V_S3 1D5V_S0

CPU V_CORE 41,42
ISL6559CR

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM POWER 44,45
FDD6035AL/FDS9412-U
FDS9412-U/SI4892DY/LP2951ACM
APL5508-18VC/APL5308-25AC

INPUT	OUTPUT
5V_S3 3D3V_S5 3D3V_S3 3D3V_S0 DCBATOUT	2D5V_S5 5V_S0 3D3V_S3 3D3V_S0 3D3V_LAN_S3 1D8V_S0 +5V_AUX_S5 +5V_UP_S5 2D5V_S0

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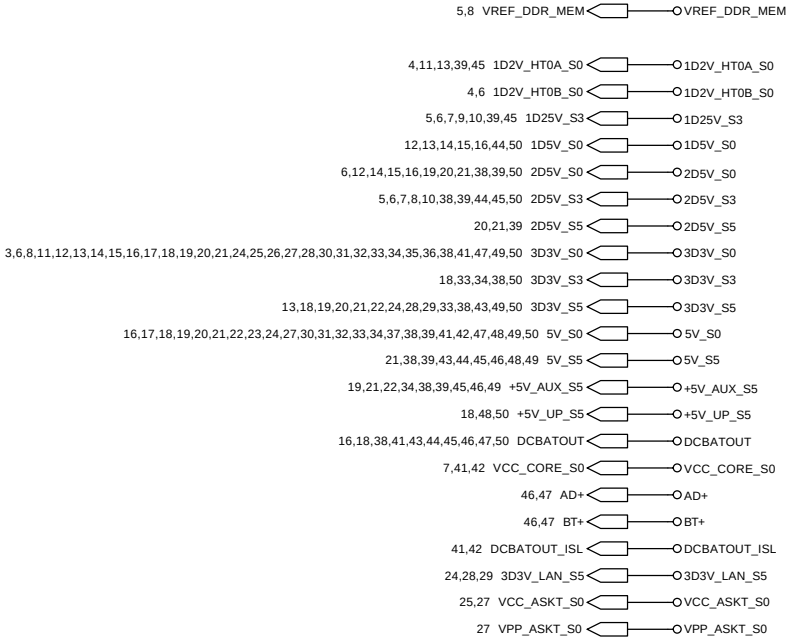
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Block Diagram		
Size A3	Document Number EGRET	Rev SC
Date: Friday, July 23, 2004	Sheet 1 of 50	

EGRET REVISION HISTORY

PCI RESOURCE TABLE

DEVICE	IDSEL	PCI IRQ	REQ# / GNT#
VGA & AGP		P_INTA#	
PCI7420-CardBus A	AD22	P_INTB#	P_REQ#1/P_GNT#1
PCI7420-CardBus B	AD22	P_INTC#	P_REQ#1/P_GNT#1
PCI7420-IEEE1394A	AD22	P_INTD#	P_REQ#1/P_GNT#1
Mini-PCI	AD21	P_INTF#	P_REQ#0/P_GNT#0
Giga LAN RTL8110SBL	AD23	P_INTG#	P_REQ#2/P_GNT#2



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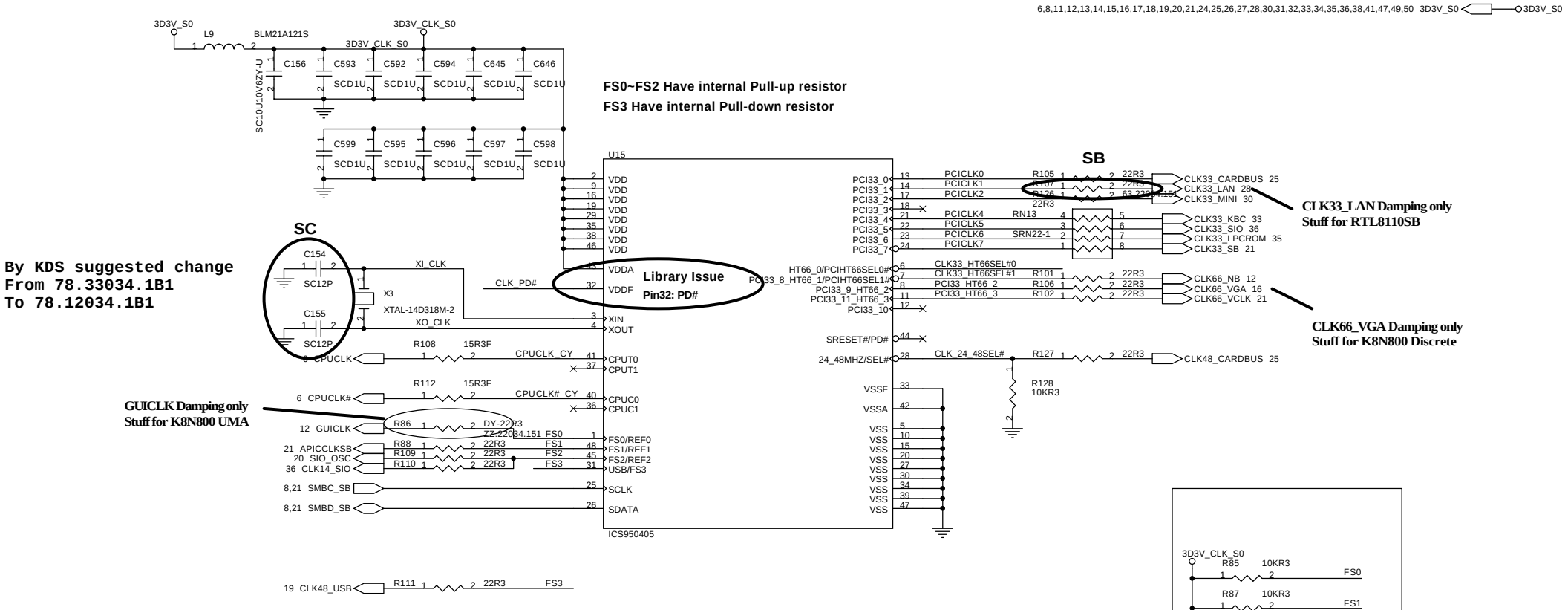
Title: REVISION HISTORY

Size: A3 | Document Number: EGRET | Rev: SC

Date: Friday, July 23, 2004 | Sheet 2 of 50



Input Configuration				Clock Generator Output			
FS3	FS2	FS1	FS0	CPU (MHz)	PCI33_HT66 (MHz)	PCI33 (MHz)	
0	0	0	0	100.90	67.27	33.63	All output Tri-state
0	0	0	1	133.90	66.95	33.48	
0	0	1	0	168.00	67.20	33.60	
0	0	1	1	202.00	67.33	33.67	
0	1	0	0	100.20	66.80	33.40	
0	1	0	1	133.50	66.75	33.38	
0	1	1	0	166.70	66.68	33.34	
* 0	1	1	1	200.40	66.80	33.40	Normal Hammer operation
1	0	0	0	150.00	60.00	30.00	
1	0	0	1	180.00	60.00	30.00	
1	0	1	0	210.00	70.00	35.00	
1	0	1	1	240.00	60.00	30.00	
1	1	0	0	270.00	67.50	33.75	
1	1	0	1	233.33	66.67	33.33	
1	1	1	0	266.67	66.67	33.33	
1	1	1	1	300.00	75.00	37.50	

	24_48 SEL#	24_48MHz
*	0	48MHz
	1	24MHz

	PCIHT66 SEL[1:0]#		PCI33_HT66[3:0]		
	SEL0	SEL1	PIN7	PIN8	PIN11
	0	0	HT66	HT66	PCI33
*	0	1	HT66	HT66	HT66
	1	0	PCI33	PCI33	PCI33
	1	1	HT66	PCI33	PCI33

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Title: ***CLKGEN_ICS950405***

Size: A3 | Document Number: **EGRET** | Rev: SC

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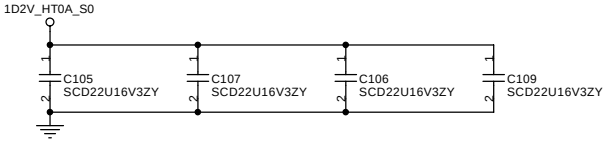
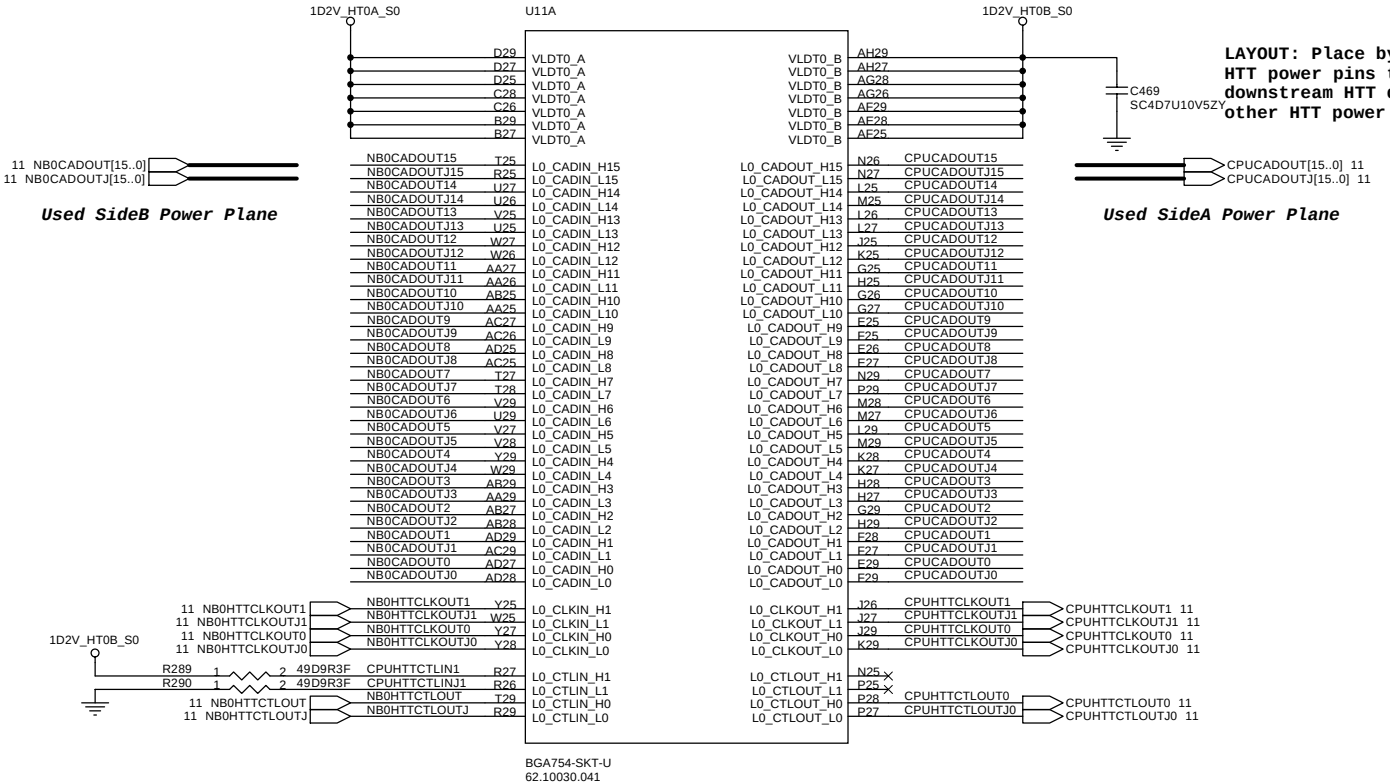


11,13,39,45 1D2V_HT0A_S0 — 1D2V_HT0A_S0

6 1D2V_HT0B_S0 — 1D2V_HT0B_S0

HTT for CPU sideA Transmit power and NB sideA Receive power

HTT for CPU sideB Receive power and NB sideA Transmit power



LAYOUT: Place bypass cap on topside of board near HTT power pins that are not connected directly to downstream HTT device, but connected internally to other HTT power pins.

Used SideB Power Plane

Used SideA Power Plane

By ME requset U11 P/N:
Main 62.10030.041
Second 62.10053.191
Third 62.10053.201

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Title		
CPU(1/4)_HyperTransport I/F		
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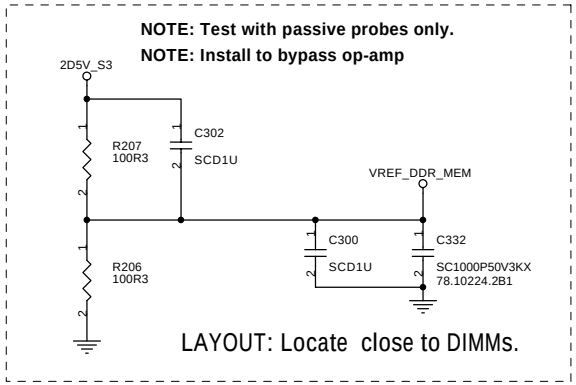
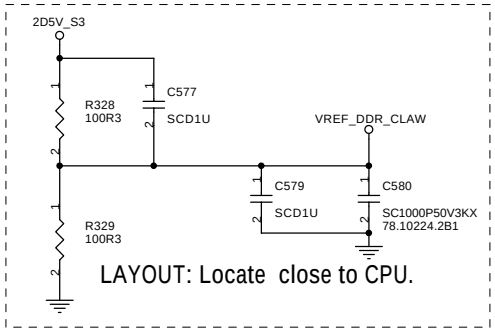
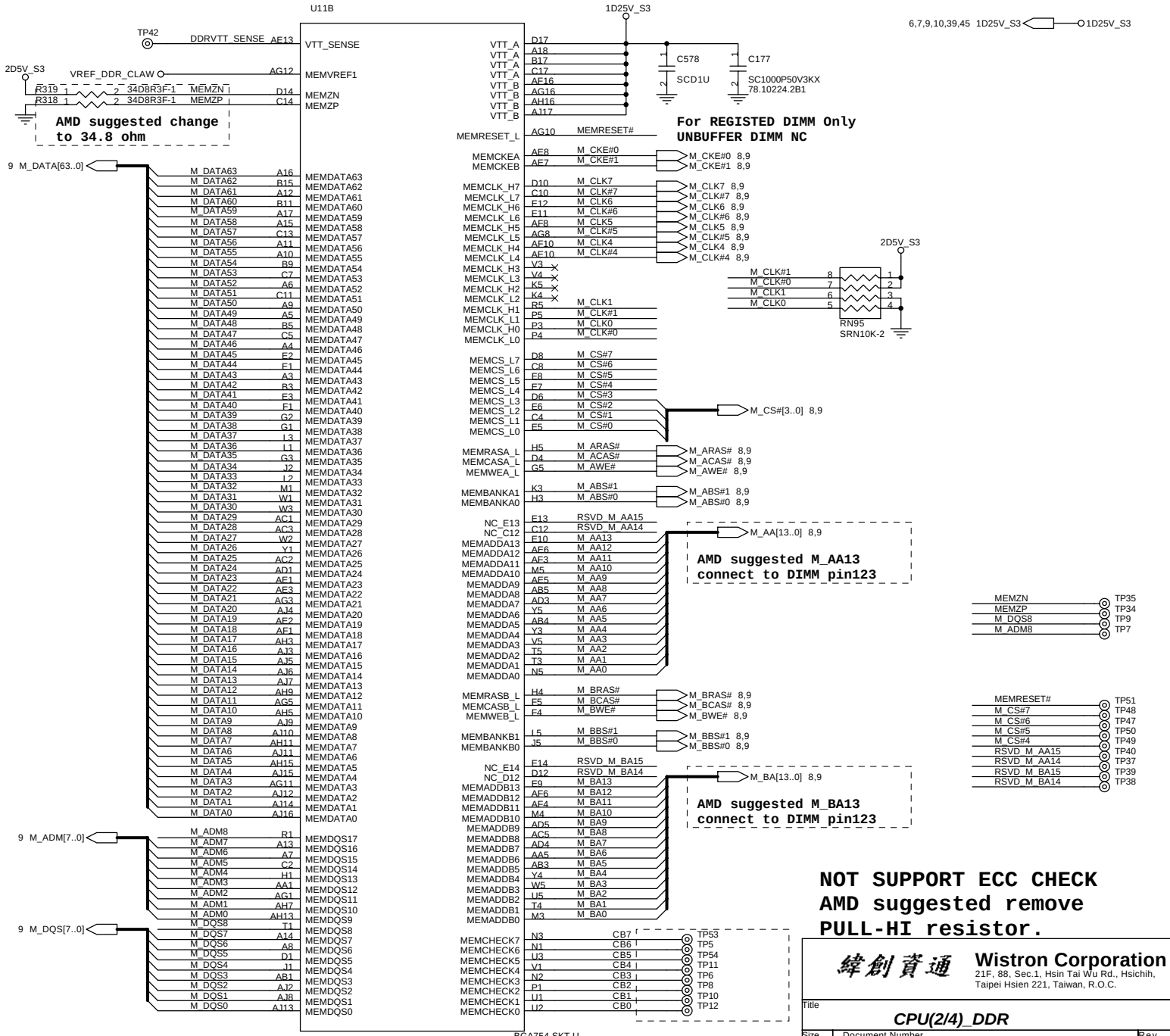
VREF_DDR_MEM



NOTE: Remove to bypass op-amp

VREF_DDR_CLAW





NOT SUPPORT ECC CHECK
AMD suggested remove
PULL-HI resistor.

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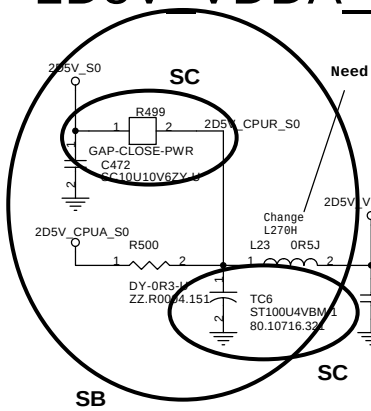
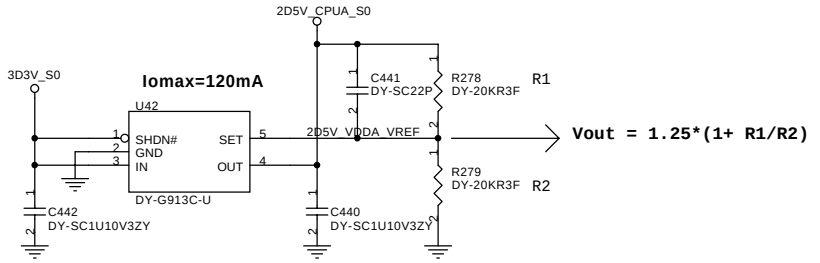
Title	*CPU(2/4)_DDR*
Size A3	Document Number **EGRET** Rev SC
Date: Friday, July 23, 2004	Sheet 5 of 50

2D5V_VDDA_S0



KEMET,NT:5.7, B2 size
ST100U4VBM-1 (80.10716.321)
Iripple=1.1A,ESR=70mohm

SANYO, NT$:6.1
Iripple=1.1A,ESR=70mohm
3.5/2.8/2.0
77.21071.031



5,7,9,10,39,45 1D25V_S3 — 1D25V_S3
12,14,15,16,19,20,21,38,39,50 2D5V_S0 — 2D5V_S0
5,7,8,10,38,39,44,45,50 2D5V_S3 — 2D5V_S3
4 1D2V_HT0B_S0 — 1D2V_HT0B_S0

LAYOUT: Route trace 50 mils wide and 500 to 750 mils long between these caps.

LAYOUT: Route VDDA trace approx. 50 mils wide (use 2x25 mil traces to exit ball field) and 500 mils long.

2D5V_VDDA_S0
C470 SC4D7U10V5ZY 78.47593.411
C471 SC3300P50V3KX
C499 SCD22U16V3ZY
1D2V_HT0B_S0
R292 44D2R3F
R291 44D2R3F
64.44R25.551
C468 SC1000P50V3KX 78.10224.2B1
C467 SC1000P50V3KX 78.10224.2B1

AMD suggest voltege from 2D5V_S0 to 2D5V_S3
differentially impedance 100

2D5V_S3
R310 820R3
R311 820R3
3 CPUCLK — C500 SC3900P50V3KX
3 CPUCLK# — C501 SC3900P50V3KX
R307 169R3F
1D25V_S3
2D5V_S0
RST_CPU# R308 680R3
ALL_PWROK R309 680R3

U11C

Pin	Signal
AH25	VDDA1
AJ25	VDDA2
AF20	RESET_L (19 RST_CPU#)
AE18	PWROK (12,19,21,39 ALL_PWROK)
AJ27	LDTSTOP_L (21 HTT_CPU_STOP#)
AF27	L0_REF1
AE26	L0_REF0
A23	COREFB (41 COREFB)
A24	COREFB# (41 COREFB#)
B23	CORE_SENSE
AE12	VDDIOFB
AE12	VDDIOFBJ
AE11	VDDIOSENSE (44 VDDIOSENSE)
AJ21	CLKIN (3 CPUCLK)
AH21	CLKIN_L
AJ23	NC_AJ23
AH23	NC_AH23
AE24	NC_AE24
AF24	NC_AF24
C16	VTT_A
AG15	VTT_B
AH17	DBRDY
C15	NC_C15
E20	TMS
F17	TCK
B21	TRST_L
A21	TDI
C18	NC_C18
A19	NC_A19
A28	KEY1
AJ28	KEY0
AE23	NC_AE23
AF23	NC_AF23
AF22	NC_AF22
AF21	NC_AF21
C1	NC_C1
J3	NC_J3
R3	NC_R3
AA2	NC_AA2
D3	NC_D3
AG2	NC_AG2
B18	NC_B18
AH1	NC_AH1
AF21	NC_AE21
C20	NC_C20
AG4	NC_AG4
C6	NC_C6
AG6	NC_AG6
AE9	NC_AE9
AG9	NC_AG9
A20	THERMTRIP_L (THERMTRIP#)
A26	THERMDA (THERMDP 22)
A27	THERMDC (THERMDN 22)
AG13	VID4
AF14	VID3
AG14	VID2
AF15	VID1
AE15	VID0
AG18	NC_AG18 (TP45)
AH18	NC_AH18 (TP46)
AG17	NC_AG17
AJ18	NC_AJ18
AH19	FBCLKOUT_H
AJ19	FBCLKOUT_L
AE19	DBREQ_L (DBREQJ)
D20	NC_D20
C21	NC_C21
D18	NC_D18
C19	NC_C19
B19	NC_B19
A22	TDO
AF18	NC_AF18
D22	NC_D22
C22	NC_C22
B13	NC_B13
B7	NC_B7
C3	NC_C3
K1	NC_K1
R2	NC_R2
AA3	NC_AA3
F3	NC_F3
C23	NC_C23
AG7	NC_AG7
AF22	NC_AE22
C24	NC_C24
A25	NC_A25
C9	NC_C9

BGA754-SKT-U

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

FBCLKOUT
R323 80D6R3F-U
FBCLKOUTJ

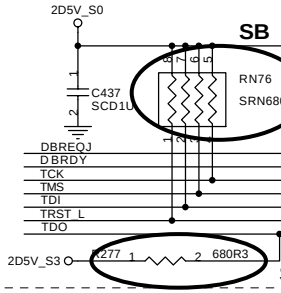
R322 DUMMY-R3

Connect to VDDIO for AMD suggest.
SB
2D5V_S3

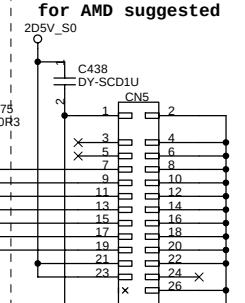
2D5V_S0
R193 680R3
THERMTRIP#
Q20 MMBT3904-U1
CPU_THERMTRIP# 38
R194 1KR3
NS3

THERMTRIPJ Level shift to VT8235
EM_OFF PIN near VT8235

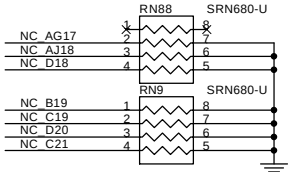
HDT Connectors



Add HDT connector for AMD suggested



CHANGE FROM 1KR3 TO 680R2 FOR AMD CHECK LIST



Validation Test Points

LAYOUT: Place close to the CPU.

NC_C15	TP36
NC_AE23	TP24
NC_AF23	TP25
NC_AF22	TP26
NC_AF21	TP27
RST_CPU#	TP30
CLKIN	TP32
CLKIN#	TP33
CORE_SENSE	TP28
VDDIOFB	TP43
VDDIOFBJ	TP44
VDDIOSENSE	TP41
NC_AE24	TP29
NC_AF24	TP31

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Title: ***CPU(3/4)_Control & Debug***

Size: A3 | Document Number: **EGRET** | Rev: SC

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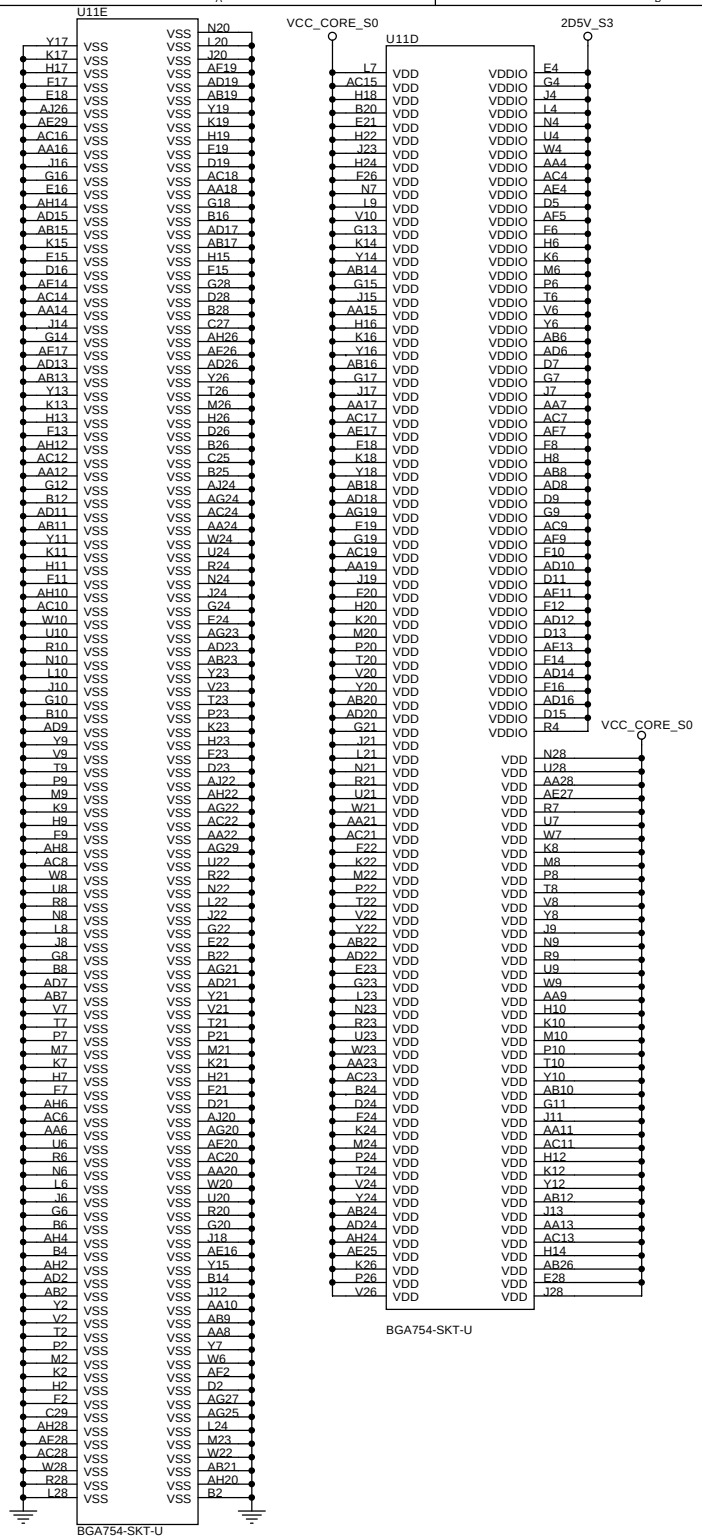

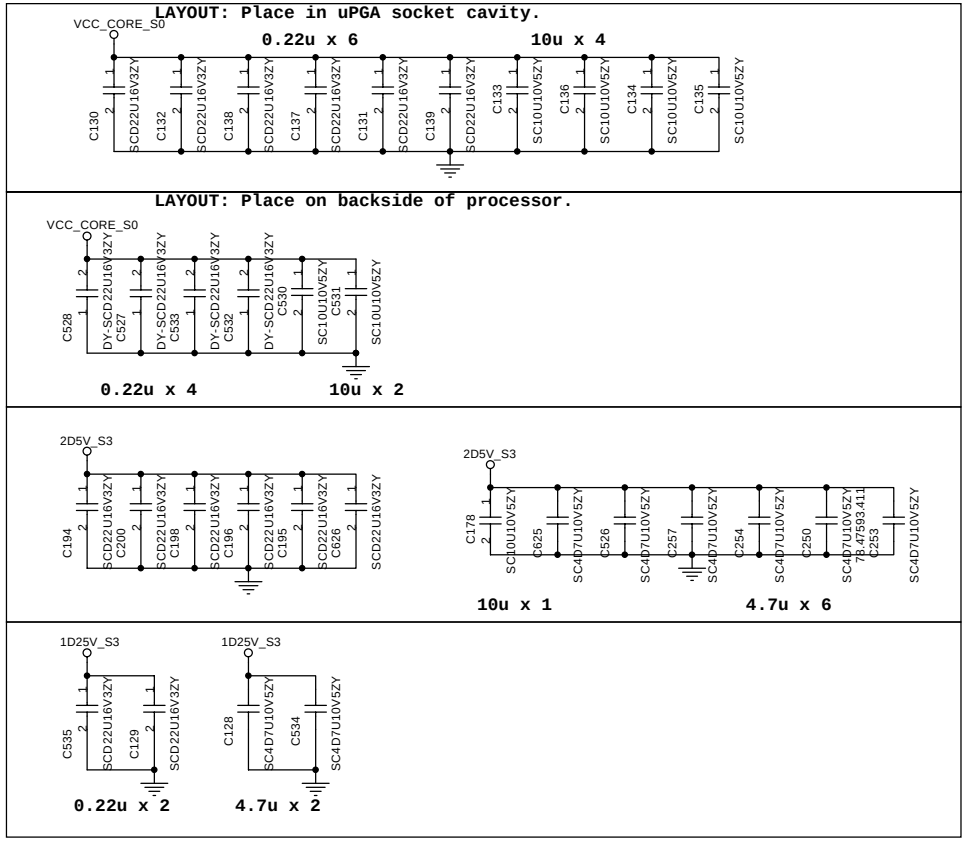

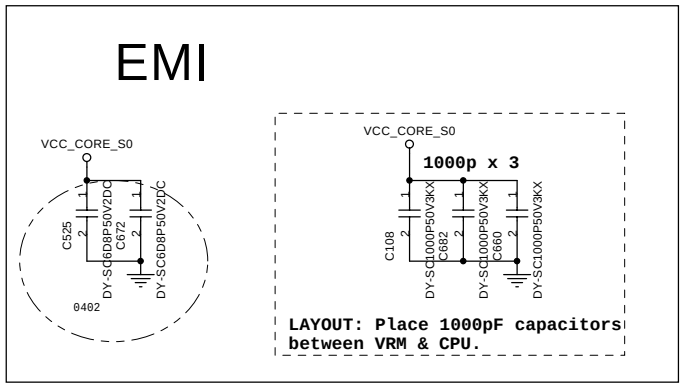

5,6,9,10,39,45 1D25V_S3 — 1D25V_S3

5,6,8,10,38,39,44,45,50 2D5V_S3 — 2D5V_S3

41,42 VCC_CORE_S0 — VCC_CORE_S0

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Title: CPU(4/4)_Power

Size: A3 | Document Number: EGRET | Rev: SC

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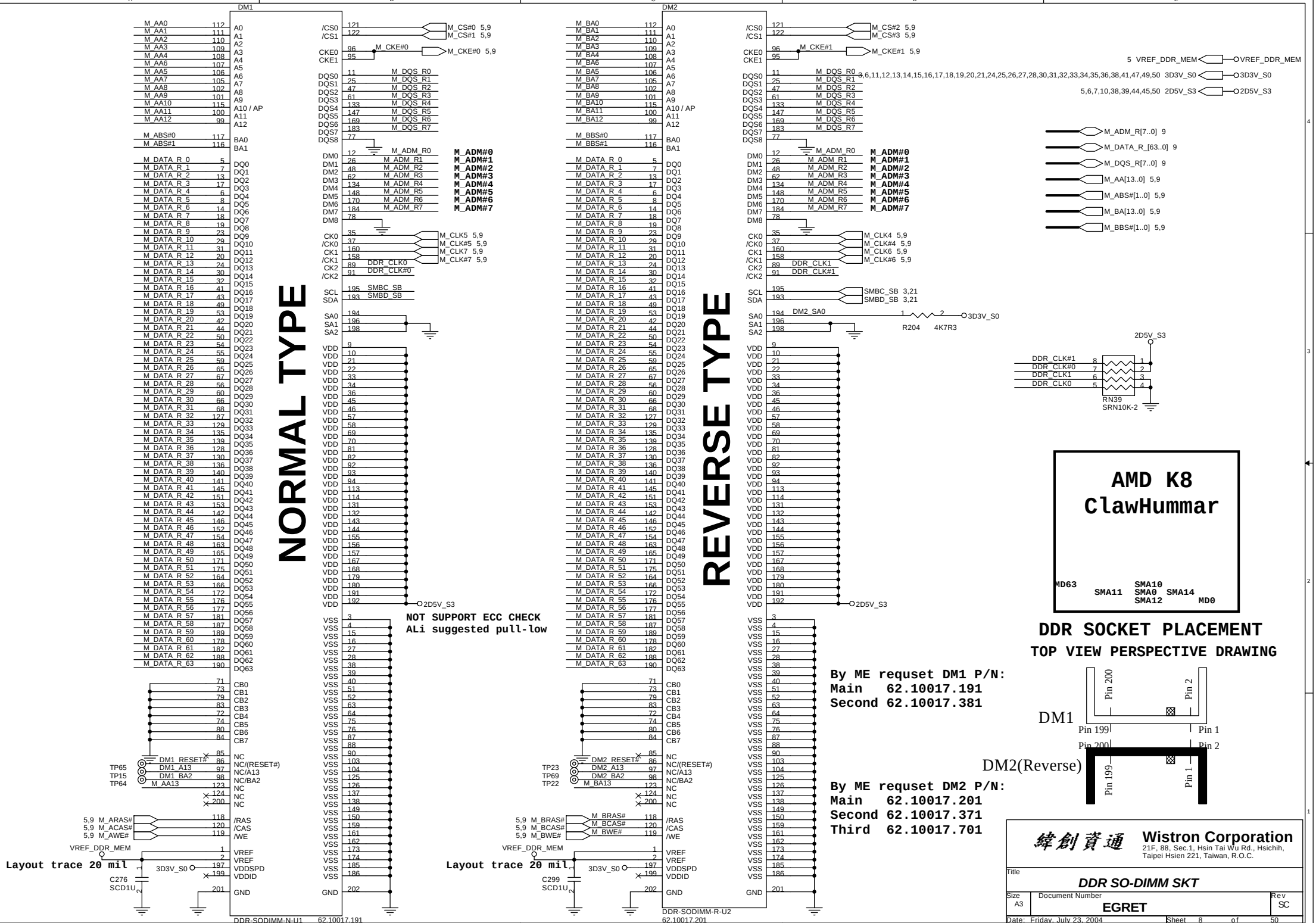
DM1
NORMAL TYPE
DM2
REVERSE TYPE
M_CS#0 5,9
M_CS#1 5,9
M_CKE#0
M_CKE#0 5,9
M_DQS_R0
M_DQS_R1
M_DQS_R2
M_DQS_R3
M_DQS_R4
M_DQS_R5
M_DQS_R6
M_DQS_R7
M_ADM_R0
M_ADM_R1
M_ADM_R2
M_ADM_R3
M_ADM_R4
M_ADM_R5
M_ADM_R6
M_ADM_R7
M_ADM#0
M_ADM#1
M_ADM#2
M_ADM#3
M_ADM#4
M_ADM#5
M_ADM#6
M_ADM#7
M_CLK5 5,9
M_CLK#5 5,9
M_CLK7 5,9
M_CLK#7 5,9
DDR_CLK0
DDR_CLK#0
SMBC_SB
SMBD_SB
2D5V_S3
NOT SUPPORT ECC CHECK
ALi suggested pull-low
M_CS#2 5,9
M_CS#3 5,9
M_CKE#1
M_CKE#1 5,9
M_CLK4 5,9
M_CLK#4 5,9
M_CLK6 5,9
M_CLK#6 5,9
DDR_CLK1
DDR_CLK#1
SMBC_SB 3,21
SMBD_SB 3,21
DM2_SA0
3D3V_S0
R204 4K7R3
VREF_DDR_MEM
3D3V_S0
2D5V_S3
M_ADM_R[7..0] 9
M_DATA_R_[63..0] 9
M_DQS_R[7..0] 9
M_AA[13..0] 5,9
M_ABS#[1..0] 5,9
M_BA[13..0] 5,9
M_BBS#[1..0] 5,9
2D5V_S3
DDR_CLK#1
DDR_CLK#0
DDR_CLK1
DDR_CLK0
RN39
SRN10K-2
AMD K8
ClawHummar
MD63
SMA11
SMA10
SMA0
SMA14
SMA12
MD0
DDR SOCKET PLACEMENT
TOP VIEW PERSPECTIVE DRAWING
DM1
Pin 200
Pin 2
Pin 199
Pin 1
DM2(Reverse)
Pin 200
Pin 2
Pin 199
Pin 1
By ME requset DM1 P/N:
Main 62.10017.191
Second 62.10017.381
By ME requset DM2 P/N:
Main 62.10017.201
Second 62.10017.371
Third 62.10017.701
Layout trace 20 mil
Layout trace 20 mil
C276
SCD1U
C299
SCD1U
DDR-SODIMM-N-U1 62.10017.191
DDR-SODIMM-R-U2
62.10017.201
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR SO-DIMM SKT
Size A3
Document Number
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Rev SC
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SERIES DAMPING

PLACE RNs CLOSE TO FIRST DM (DM1), < 0.75"
STRICT EQUAL LENGTH LIMITATION WITH DQS,
CB PINS

RN23 (SRN10J-3)

M_DATA4	1	16	M_DATA_R_4
M_DATA5	2	15	M_DATA_R_5
M_ADM0	3	14	M_ADM_R0
M_DATA6	4	13	M_DATA_R_6
M_DATA7	5	12	M_DATA_R_7
M_DATA13	6	11	M_DATA_R_13
M_DATA12	7	10	M_DATA_R_12
M_ADM1	8	9	M_ADM_R1

RN20 (SRN10J-3)

M_DATA34	1	16	M_DATA_R_34
M_DATA32	2	15	M_DATA_R_32
M_DQS4	3	14	M_DQS_R4
M_DATA33	4	13	M_DATA_R_33
M_DATA36	5	12	M_DATA_R_36
M_DATA37	6	11	M_DATA_R_37
M_ADM4	7	10	M_ADM_R4
M_DATA39	8	9	M_DATA_R_39

RN44 (SRN10J-3)

M_DATA1	1	16	M_DATA_R_1
M_DATA0	2	15	M_DATA_R_0
M_DQS0	3	14	M_DQS_R0
M_DATA2	4	13	M_DATA_R_2
M_DATA3	5	12	M_DATA_R_3
M_DATA8	6	11	M_DATA_R_8
M_DATA9	7	10	M_DATA_R_9
M_DQS1	8	9	M_DQS_R1

RN32 (SRN10J-3)

M_DATA35	1	16	M_DATA_R_35
M_DATA41	2	15	M_DATA_R_41
M_DATA40	3	14	M_DATA_R_40
M_DQS5	4	13	M_DQS_R5
M_DATA42	5	12	M_DATA_R_42
M_DATA43	6	11	M_DATA_R_43
M_DATA49	7	10	M_DATA_R_49
M_DATA48	8	9	M_DATA_R_48

RN22 (SRN10J-3)

M_DATA14	1	16	M_DATA_R_14
M_DATA15	2	15	M_DATA_R_15
M_DATA21	3	14	M_DATA_R_21
M_DATA20	4	13	M_DATA_R_20
M_ADM2	5	12	M_ADM_R2
M_DATA23	6	11	M_DATA_R_23
M_DATA22	7	10	M_DATA_R_22
M_DATA25	8	9	M_DATA_R_25

RN19 (SRN10J-3)

M_DATA38	1	16	M_DATA_R_38
M_DATA45	2	15	M_DATA_R_45
M_DATA44	3	14	M_DATA_R_44
M_ADM5	4	13	M_ADM_R5
M_DATA47	5	12	M_DATA_R_47
M_DATA46	6	11	M_DATA_R_46
M_DATA53	7	10	M_DATA_R_53
M_DATA52	8	9	M_DATA_R_52

RN42 (SRN10J-3)

M_DATA11	1	16	M_DATA_R_11
M_DATA10	2	15	M_DATA_R_10
M_DATA17	3	14	M_DATA_R_17
M_DATA16	4	13	M_DATA_R_16
M_DQS2	5	12	M_DQS_R2
M_DATA19	6	11	M_DATA_R_19
M_DATA18	7	10	M_DATA_R_18
M_DATA24	8	9	M_DATA_R_24

RN29 (SRN10J-3)

M_DQS6	1	16	M_DQS_R6
M_DATA50	2	15	M_DATA_R_50
M_DATA51	3	14	M_DATA_R_51
M_DATA56	4	13	M_DATA_R_56
M_DATA57	5	12	M_DATA_R_57
M_DQS7	6	11	M_DQS_R7
M_DATA58	7	10	M_DATA_R_58
M_DATA59	8	9	M_DATA_R_59

RN21 (SRN10J-3)

M_DATA29	1	16	M_DATA_R_29
M_DATA28	2	15	M_DATA_R_28
M_DQS3	3	14	M_DQS_R3
M_ADM3	4	13	M_ADM_R3
M_DATA26	5	12	M_DATA_R_26
M_DATA27	6	11	M_DATA_R_27
M_DATA30	7	10	M_DATA_R_30
M_DATA31	8	9	M_DATA_R_31

RN18 (SRN10J-3)

M_ADM6	1	16	M_ADM_R6
M_DATA54	2	15	M_DATA_R_54
M_DATA55	3	14	M_DATA_R_55
M_DATA61	4	13	M_DATA_R_61
M_DATA60	5	12	M_DATA_R_60
M_ADM7	6	11	M_ADM_R7
M_DATA62	7	10	M_DATA_R_62
M_DATA63	8	9	M_DATA_R_63

5,8 M_CKE#0 — M_CKE#0
5,8 M_CKE#1 — M_CKE#1

05/10
Remove the damping resistor for AMD suggest.

PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO SECOND DM (DM2)
NO EQUAL LENGTH LIMITATION

5,6,7,10,39,45 1D25V_S3 — 1D25V_S3

1D25V_S3

RN45 / RN33

M_ADM_R1	1	16	1	16	M_DATA_R_36
M_DATA_R_13	2	15	2	15	M_DATA_R_32
M_DATA_R_12	3	14	3	14	M_DATA_R_37
M_DATA_R_6	4	13	4	13	M_DATA_R_33
M_DATA_R_7	5	12	5	12	M_ADM_R4
M_ADM_R0	6	11	6	11	M_DQS_R4
M_DATA_R_5	7	10	7	10	M_DATA_R_38
M_DATA_R_4	8	9	8	9	M_DATA_R_39

SRN68J-1 RN65 / SRN68J-1 RN61

M_DATA_R_1	1	16	1	16	M_DATA_R_48
M_DATA_R_0	2	15	2	15	M_DATA_R_49
M_DQS_R0	3	14	3	14	M_DATA_R_43
M_DATA_R_2	4	13	4	13	M_DATA_R_42
M_DATA_R_3	5	12	5	12	M_DQS_R5
M_DATA_R_8	6	11	6	11	M_DATA_R_41
M_DATA_R_9	7	10	7	10	M_DATA_R_40
M_DQS_R1	8	9	8	9	M_DATA_R_34

SRN68J-1 RN43 / SRN68J-1 RN31

M_DATA_R_25	1	16	1	16	M_DATA_R_35
M_DATA_R_22	2	15	2	15	M_DATA_R_46
M_DATA_R_23	3	14	3	14	M_DATA_R_47
M_ADM_R2	4	13	4	13	M_ADM_R5
M_DATA_R_20	5	12	5	12	M_DATA_R_44
M_DATA_R_21	6	11	6	11	M_DATA_R_45
M_DATA_R_14	7	10	7	10	M_DATA_R_53
M_DATA_R_15	8	9	8	9	M_DATA_R_52

SRN68J-1 RN64 / SRN68J-1 RN60

M_DATA_R_11	1	16	1	16	M_DATA_R_59
M_DATA_R_10	2	15	2	15	M_DATA_R_58
M_DATA_R_16	3	14	3	14	M_DQS_R7
M_DATA_R_17	4	13	4	13	M_DATA_R_57
M_DQS_R2	5	12	5	12	M_DATA_R_56
M_DATA_R_19	6	11	6	11	M_DATA_R_51
M_DATA_R_18	7	10	7	10	M_DATA_R_50
M_DATA_R_24	8	9	8	9	M_DQS_R6

SRN68J-1 RN41 / SRN68J-1 RN30

M_DATA_R_30	1	16	1	16	M_DATA_R_55
M_DATA_R_31	2	15	2	15	M_DATA_R_54
M_DATA_R_26	3	14	3	14	M_ADM_R6
M_DATA_R_27	4	13	4	13	M_DATA_R_60
M_ADM_R3	5	12	5	12	M_DATA_R_61
M_DQS_R3	6	11	6	11	M_ADM_R7
M_DATA_R_29	7	10	7	10	M_DATA_R_63
M_DATA_R_28	8	9	8	9	M_DATA_R_62

SRN68J-1 / SRN68J-1

1D25V_S3

RN63

M_CKE#1	2	3	
M_BA12	1	4	

SRN47J RN40

M_CKE#0	2	3	
M_AA12	1	4	

SRN47J RN37

M_AA11	1	16	
M_AA9	2	15	
M_AA7	3	14	
M_AA5	4	13	
M_AA4	5	12	
M_AA8	6	11	
M_AA6	7	10	
M_AA3	8	9	

SRN47J-1-U RN36

M_CS#3	1	16	
M_BA13	2	15	
M_CS#2	3	14	
M_BRAS#	4	13	
M_BBS#1	5	12	
M_BCAS#	6	11	
M_BA0	7	10	
M_BA2	8	9	

SRN47J-1-U RN35

M_AA1	1	16	
M_AA10	2	15	
M_AA2	3	14	
M_AA0	4	13	
M_ABS#1	5	12	
M_ARAS#	6	11	
M_AWE#	7	10	
M_ABS#0	8	9	

SRN47J-1-U RN62

M_BA7	1	16	
M_BA3	2	15	
M_BA6	3	14	
M_BA9	4	13	
M_BA10	5	12	
M_BA1	6	11	
M_BBS#0	7	10	
M_BWE#	8	9	

SRN47J-1-U RN38 (SRN47-1)

M_BA5	1	8
M_BA8	2	7
M_BA11	3	6
M_BA4	4	5

RN34 (SRN47-1)

M_AA13	1	8
M_CS#0	2	7
M_CS#1	3	6
M_ACAS#	4	5

M_ADM_R[7..0] 8
M_ADM[7..0] 5
M_DATA[63..0] 5
M_DATA_R_[63..0] 8
M_DQS[7..0] 5
M_DQS_R[7..0] 8
M_AA[13..0] 5,8
M_ABS#[1..0] 5,8
M_BA[13..0] 5,8
M_BBS#[1..0] 5,8
M_AWE# 5,8
M_ACAS# 5,8
M_ARAS# 5,8
M_BWE# 5,8
M_BCAS# 5,8
M_BRAS# 5,8
M_CS#0 5,8
M_CS#1 5,8
M_CS#2 5,8
M_CS#3 5,8

PLACE BETWEEN DM1, DM2
CLOSE TO FIRST DM (DM 2) < 0.2", TO SECOND DM (DM1) < 1.1"
EQUAL LENGTH LIMITATION WITH SCK/SCK#

R171 121R3F — M_CLK7 — M_CLK7 5,8 / M_CLK#7 5,8
R239 121R3F — M_CLK6 — M_CLK6 5,8 / M_CLK#6 5,8
R205 121R3F — M_CLK5 — M_CLK5 5,8 / M_CLK#5 5,8
R240 121R3F — M_CLK4 — M_CLK4 5,8 / M_CLK#4 5,8

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR DAMPING & TERMINATION**

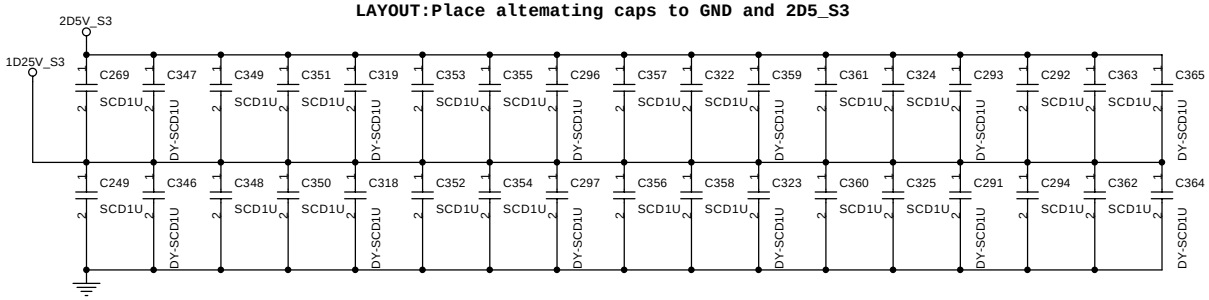
Size	Document Number	Rev
A3	EGRET	SC

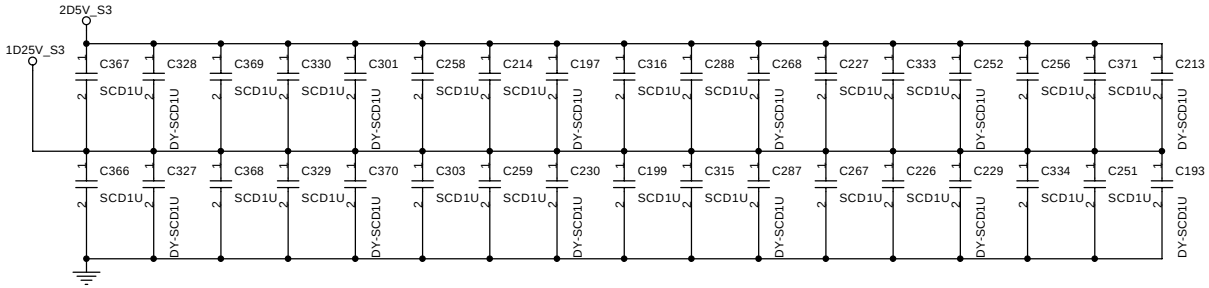
Date: Friday, July 23, 2004 Sheet 9 of 50

5,6,7,8,38,39,44,45,50 2D5V_S3 — 2D5V_S3

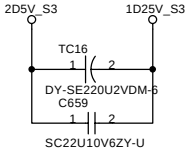
5,6,7,9,39,45 1D25V_S3 — 1D25V_S3

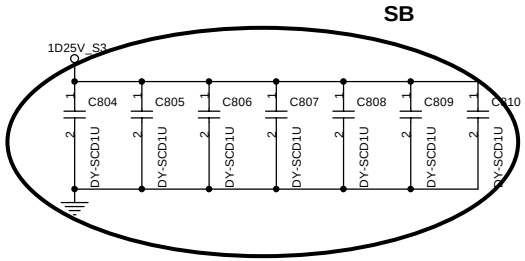
LAYOUT:Place altemating caps to GND and 2D5_S3



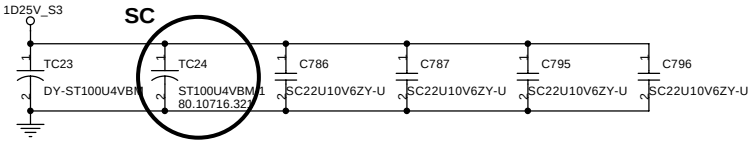


LAYOUT:Locate close to CPU socket.





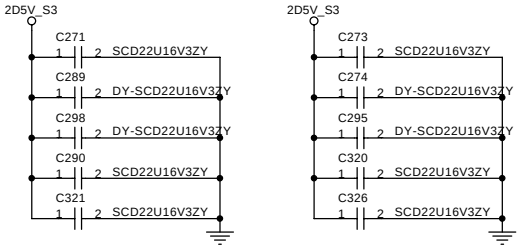
LAYOUT:Place at end of the DIMMs



KEMET,NT:5.7, B2 size
ST100U4VBM-1 (80.10716.321)
Iripple=1.1A,ESR=70mohm

SANYO, NT$:6.1
Iripple=1.1A,ESR=70mohm
3.5/2.8/2.0
77.21071.031

LAYOUT:Place close to Power Pin of DDR socket.



0.22u x 10

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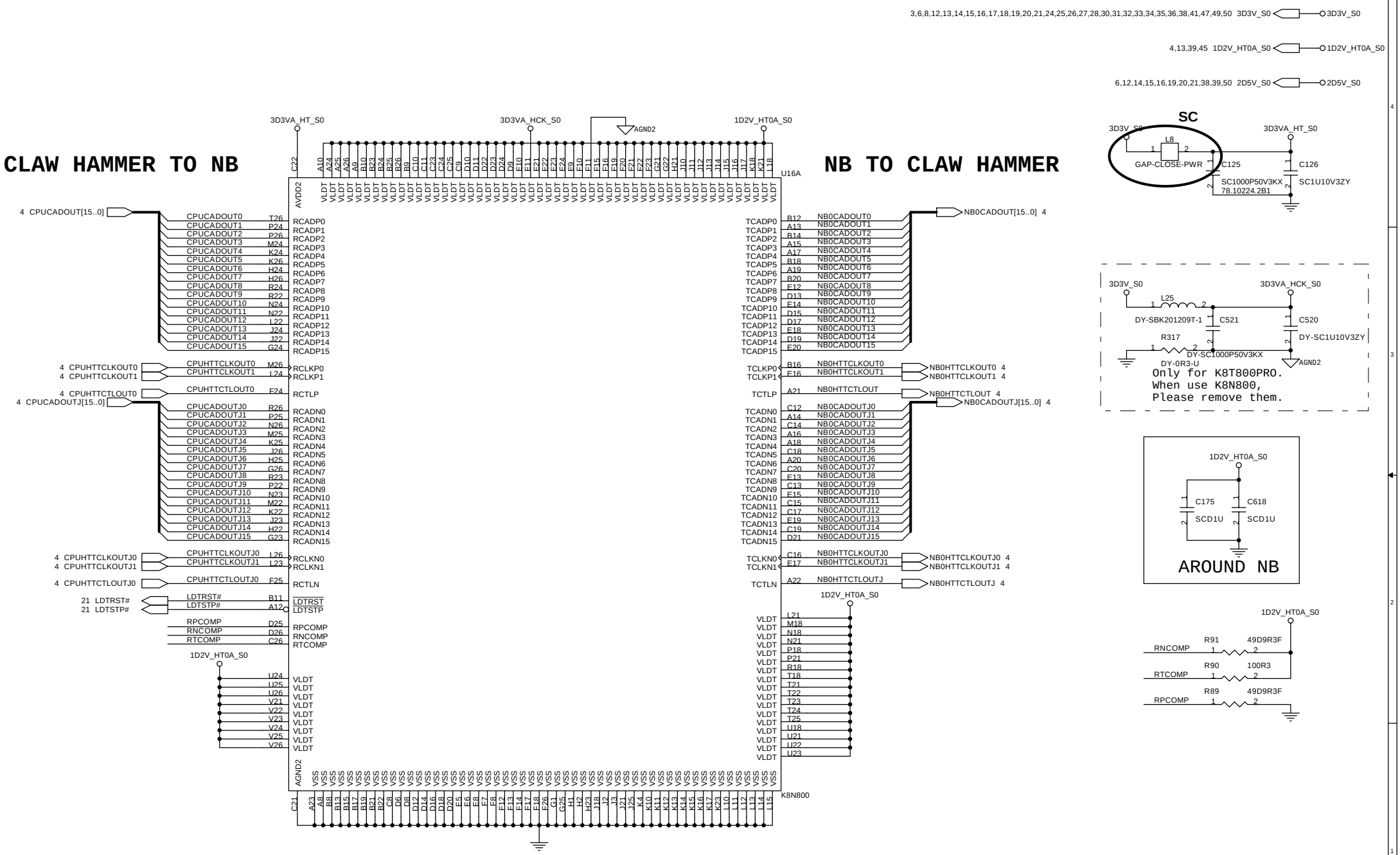
Title: ***DDR DECOUPLING***

Size: A3 | Document Number: **EGRET** | Rev: SC

Date: Friday, July 23, 2004 | Sheet 10 of 50



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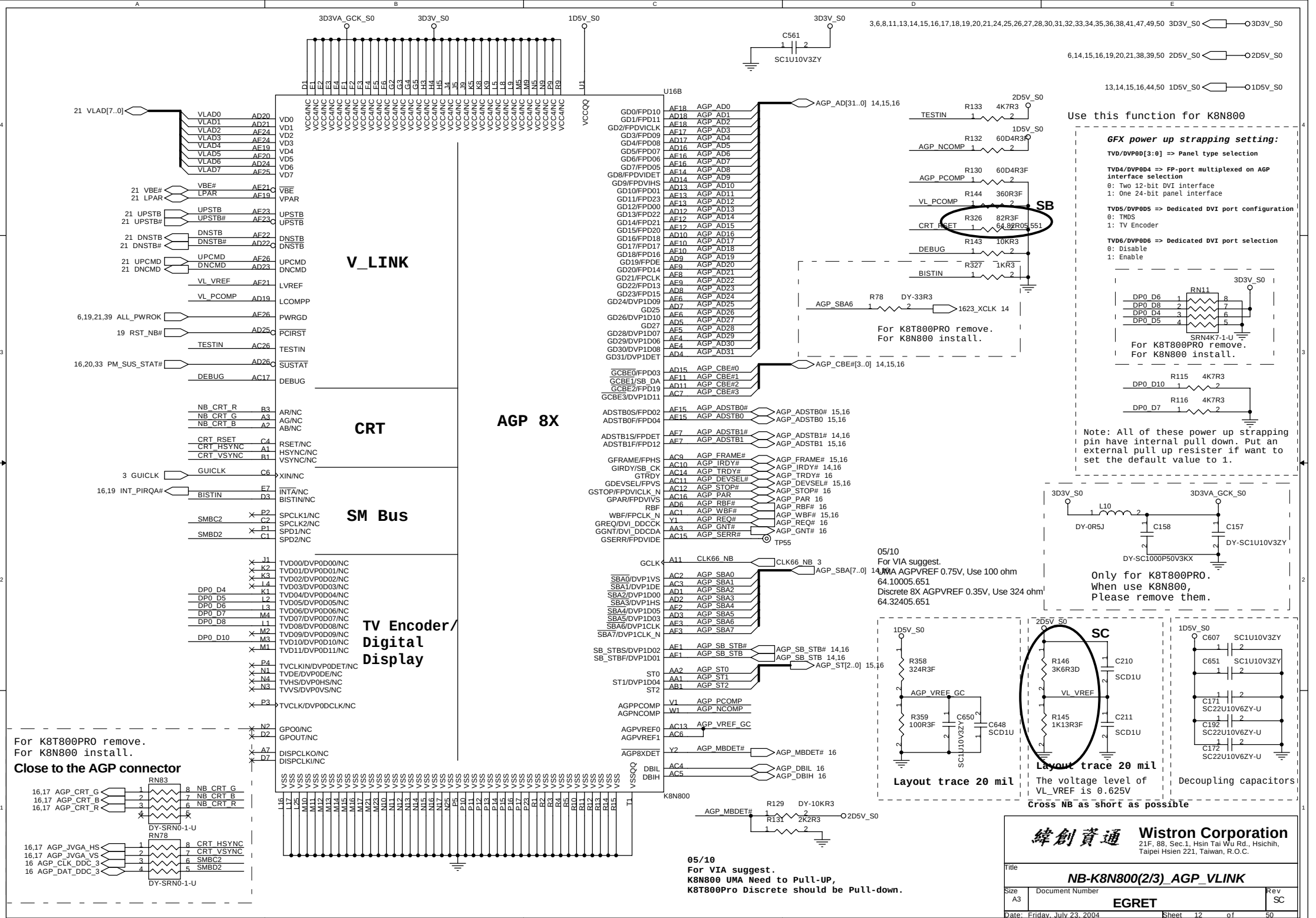
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***NB-K8N800(1/3)_HT***

Size: A3 | Document Number: **EGRET** | Rev: SC

Date: Friday, July 23, 2004 | Sheet 11 of 50


3D3VA_GCK_S0
3D3V_S0
1D5V_S0
U16B
V_LINK
CRT
AGP 8X
SM Bus
TV Encoder/ Digital Display
K8N800
21 VLAD[7..0]
VLAD0 AD20 VD0
VLAD1 AD21 VD1
VLAD2 AE24 VD2
VLAD3 AE24 VD3
VLAD4 AE19 VD4
VLAD5 AE20 VD5
VLAD6 AD24 VD6
VLAD7 AE25 VD7
21 VBE# AE21 VBE
21 LPAR AE19 VPAR
21 UPSTB AE23 UPSTB
21 UPSTB# AE23 UPSTB
21 DNSTB AE22 DNSTB
21 DNSTB# AD22 DNSTB
21 UPCMD AE26 UPCMD
21 DNCMD AD23 DNCMD
VL_VREF AE21 LVREF
VL_PCOMP AD19 LCOMPP
6,19,21,39 ALL_PWROK AE26 PWRGD
19 RST_NB# AD25 PCIRST
TESTIN AC26 TESTIN
16,20,33 PM_SUS_STAT# AD26 SUSTAT
DEBUG AC17 DEBUG
NB_CRT_R B3 AR/NC
NB_CRT_G A3 AG/NC
NB_CRT_B A2 AB/NC
CRT_RSET C4 RSET/NC
CRT_HSYNC A1 HSYNC/NC
CRT_VSYNC B1 VSYNC/NC
3 GUICLK C6 XIN/NC
16,19 INT_PIRQA# E7 INTA/NC
BISTIN D3 BISTIN/NC
SMBC2 P2 SPCLK1/NC
C2 SPCLK2/NC
SMBD2 P1 SPD1/NC
C1 SPD2/NC
DP0_D4 J1 TVD00/DVP0D00/NC
DP0_D5 K2 TVD01/DVP0D01/NC
DP0_D6 K3 TVD02/DVP0D02/NC
DP0_D7 L4 TVD03/DVP0D03/NC
DP0_D8 K1 TVD04/DVP0D04/NC
L2 TVD05/DVP0D05/NC
L3 TVD06/DVP0D06/NC
M4 TVD07/DVP0D07/NC
L1 TVD08/DVP0D08/NC
DP0_D10 M2 TVD09/DVP0D09/NC
M3 TVD10/DVP0D10/NC
M1 TVD11/DVP0D11/NC
P4 TVCLKIN/DVP0DET/NC
N1 TVDE/DVP0DE/NC
N4 TVHS/DVP0HS/NC
N3 TVVS/DVP0VS/NC
P3 TVCLK/DVP0DCLK/NC
N2 GPO0/NC
D2 GPOUT/NC
A7 DISPCLKO/NC
D7 DISPCLKI/NC
GD0/FPD10 AF18 AGP_AD0
GD1/FPD11 AD18 AGP_AD1
GD2/FPDVICLK AE18 AGP_AD2
GD3/FPD09 AE17 AGP_AD3
GD4/FPD08 AD17 AGP_AD4
GD5/FPD07 AD16 AGP_AD5
GD6/FPD06 AE16 AGP_AD6
GD7/FPD05 AF16 AGP_AD7
GD8/FPDVIDET AE14 AGP_AD8
GD9/FPDVIHS AD14 AGP_AD9
GD10/FPD01 AD13 AGP_AD10
GD11/FPD23 AE13 AGP_AD11
GD12/FPD00 AF13 AGP_AD12
GD13/FPD22 AD12 AGP_AD13
GD14/FPD21 AF12 AGP_AD14
GD15/FPD20 AE12 AGP_AD15
GD16/FPD18 AD10 AGP_AD16
GD17/FPD17 AE10 AGP_AD17
GD18/FPD16 AF10 AGP_AD18
GD19/FPDE AD9 AGP_AD19
GD20/FPD14 AF9 AGP_AD20
GD21/FPCLK AF8 AGP_AD21
GD22/FPD13 AF9 AGP_AD22
GD23/FPD15 AD8 AGP_AD23
GD24/DVP1D09 AF6 AGP_AD24
GD25 AD7 AGP_AD25
GD26/DVP1D10 AF6 AGP_AD26
GD27 AD5 AGP_AD27
GD28/DVP1D07 AF5 AGP_AD28
GD29/DVP1D06 AF4 AGP_AD29
GD30/DVP1D08 AE4 AGP_AD30
GD31/DVP1DET AD4 AGP_AD31
GCBE0/FPD03 AD15 AGP_CBE#0
GCBE1/SB_DA AE11 AGP_CBE#1
GCBE2/FPD19 AD11 AGP_CBE#2
GCBE3/DVP1D11 AC7 AGP_CBE#3
ADSTB0S/FPD02 AE15 AGP_ADSTB0#
ADSTB0F/FPD04 AE15 AGP_ADSTB0
ADSTB1S/FPDET AF7 AGP_ADSTB1#
ADSTB1F/FPD12 AF7 AGP_ADSTB1
GFRAME/FPHS AC9 AGP_FRAME#
GIRDY/SB_CK AC10 AGP_IRDY#
GTRDY AC14 AGP_TRDY#
GDEVSEL/FPVS AC11 AGP_DEVSEL#
GSTOP/FPDVICLK_N AC12 AGP_STOP#
GPAR/FPDVIVS AC16 AGP_PAR
RBF AD6 AGP_RBF#
WBF/FPCLK_N AC1 AGP_WBF#
GREQ/DVI_DDCCK Y1 AGP_REQ#
GGNT/DVI_DDCDA AA3 AGP_GNT#
GSERR/FPDVIDE AC15 AGP_SERR#
GCLK A11 CLK66_NB
SBA0/DVP1VS AC2 AGP_SBA0
SBA1/DVP1DE AC3 AGP_SBA1
SBA2/DVP1D00 AD1 AGP_SBA2
SBA3/DVP1HS AD2 AGP_SBA3
SBA4/DVP1D05 AF2 AGP_SBA4
SBA5/DVP1D03 AD3 AGP_SBA5
SBA6/DVP1CLK AE3 AGP_SBA6
SBA7/DVP1CLK_N AF3 AGP_SBA7
SB_STBS/DVP1D02 AE1 AGP_SB_STB#
SB_STBF/DVP1D01 AF1 AGP_SB_STB
ST0 AA2 AGP_ST0
ST1/DVP1D04 AA1 AGP_ST1
ST2 AB1 AGP_ST2
AGPPCOMP V1 AGP_PCOMP
AGPNCOMP W1 AGP_NCOMP
AGPVREF0 AC13 AGP_VREF_GC
AGPVREF1 AC6
AGP8XDET Y2 AGP_MBDET#
DBIL AC4
DBIH AC5
AGP_AD[31..0] 14,15,16
AGP_CBE#[3..0] 14,15,16
AGP_ADSTB0# 15,16
AGP_ADSTB0 15,16
AGP_ADSTB1# 14,16
AGP_ADSTB1 15,16
AGP_FRAME# 15,16
AGP_IRDY# 14,16
AGP_TRDY# 16
AGP_DEVSEL# 15,16
AGP_STOP# 16
AGP_PAR 16
AGP_RBF# 16
AGP_WBF# 15,16
AGP_REQ# 16
AGP_GNT# 16
TP55
CLK66_NB 3
AGP_SBA[7..0] 14,16
AGP_SB_STB# 14,16
AGP_SB_STB 14,16
AGP_ST[2..0] 15,16
AGP_MBDET# 16
AGP_DBIL 16
AGP_DBIH 16
C561 SC1U10V3ZY
3,6,8,11,13,14,15,16,17,18,19,20,21,24,25,26,27,28,30,31,32,33,34,35,36,38,41,47,49,50 3D3V_S0
6,14,15,16,19,20,21,38,39,50 2D5V_S0
13,14,15,16,44,50 1D5V_S0
TESTIN R133 4K7R3
AGP_NCOMP R132 60D4R3F
AGP_PCOMP R130 60D4R3F
VL_PCOMP R144 360R3F
CRT_RSET R326 82R3F
64.82R05.551
DEBUG R143 10KR3
BISTIN R327 1KR3
SB
AGP_SBA6 R78 DY-33R3
1623_XCLK 14
For K8T800PRO remove.
For K8N800 install.
Use this function for K8N800
GFX power up strapping setting:
TVD/DVP0D[3:0] => Panel type selection
TVD4/DVP0D4 => FP-port multiplexed on AGP interface selection
0: Two 12-bit DVI interface
1: One 24-bit panel interface
TVD5/DVP0D5 => Dedicated DVI port configuration
0: TMDS
1: TV Encoder
TVD6/DVP0D6 => Dedicated DVI port selection
0: Disable
1: Enable
RN11 SRN4K7-1-U
DP0_D6
DP0_D8
DP0_D4
DP0_D5
For K8T800PRO remove.
For K8N800 install.
R115 4K7R3 DP0_D10
R116 4K7R3 DP0_D7
Note: All of these power up strapping pin have internal pull down. Put an external pull up resister if want to set the default value to 1.
L10 DY-0R5J
C158 DY-SC1000P50V3KX
C157 DY-SC1U10V3ZY
Only for K8T800PRO.
When use K8N800,
Please remove them.
05/10
For VIA suggest.
UMA AGPVREF 0.75V, Use 100 ohm
64.10005.651
Discrete 8X AGPVREF 0.35V, Use 324 ohm
64.32405.651
R358 324R3F
R359 100R3F
C650 SC1U10V3ZY
C648 SCD1U
Layout trace 20 mil
SC
R146 3K6R3D
R145 1K13R3F
C210 SCD1U
C211 SCD1U
Layout trace 20 mil
The voltage level of VL_VREF is 0.625V
Cross NB as short as possible
C607 SC1U10V3ZY
C651 SC1U10V3ZY
C171 SC22U10V6ZY-U
C192 SC22U10V6ZY-U
C172 SC22U10V6ZY-U
Decoupling capacitors
For K8T800PRO remove.
For K8N800 install.
Close to the AGP connector
RN83 DY-SRN0-1-U
16,17 AGP_CRT_G NB_CRT_G
16,17 AGP_CRT_B NB_CRT_B
16,17 AGP_CRT_R NB_CRT_R
RN78 DY-SRN0-1-U
16,17 AGP_JVGA_HS CRT_HSYNC
16,17 AGP_JVGA_VS CRT_VSYNC
16 AGP_CLK_DDC_3 SMBC2
16 AGP_DAT_DDC_3 SMBD2
AGP_MBDET# R129 DY-10KR3
R131 2K2R3
2D5V_S0
05/10
For VIA suggest.
K8N800 UMA Need to Pull-UP,
K8T800Pro Discrete should be Pull-down.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
NB-K8N800(2/3)_AGP_VLINK
Size A3
Document Number
EGRET
Rev SC
Date: Friday, July 23, 2004
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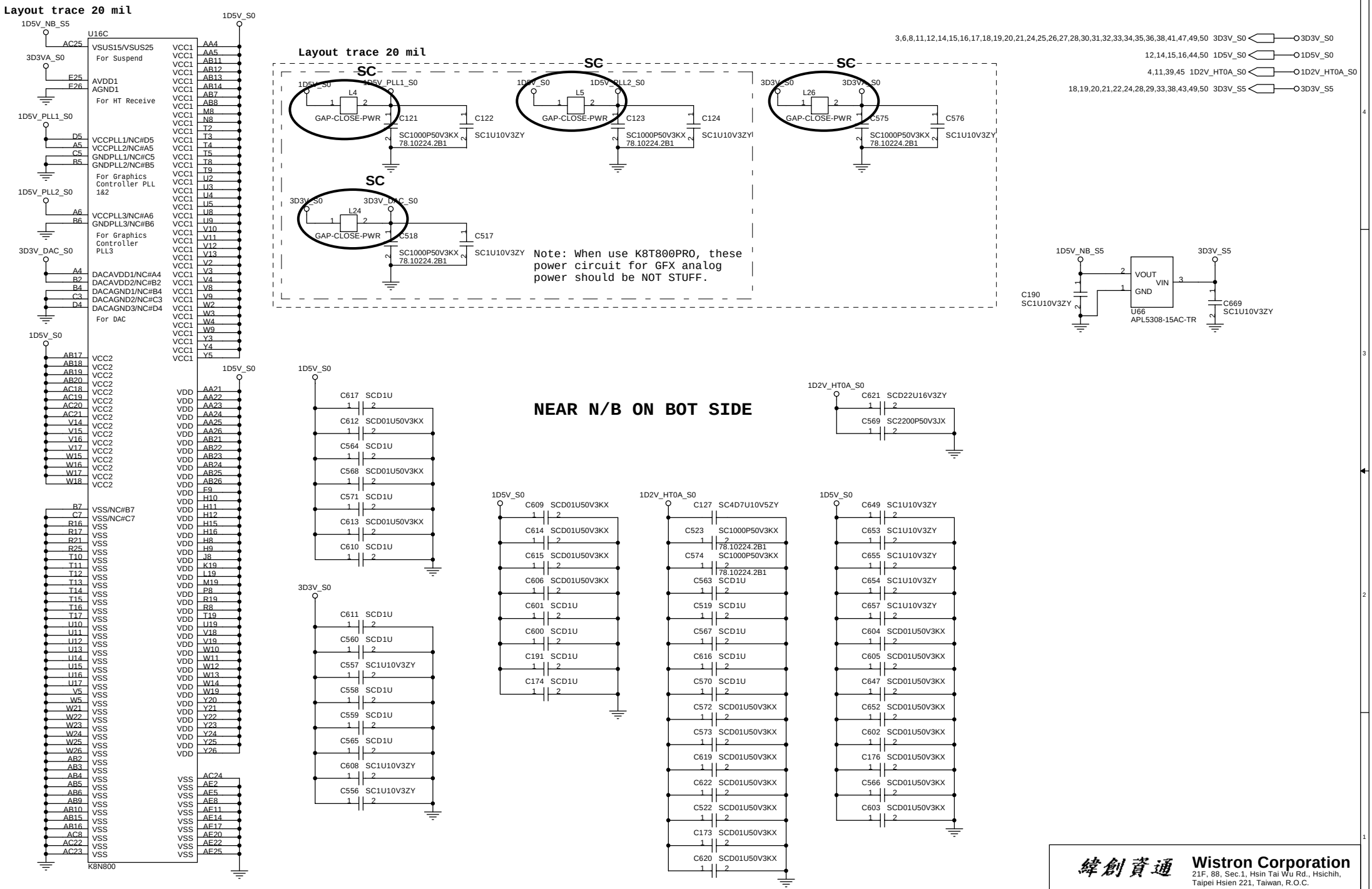
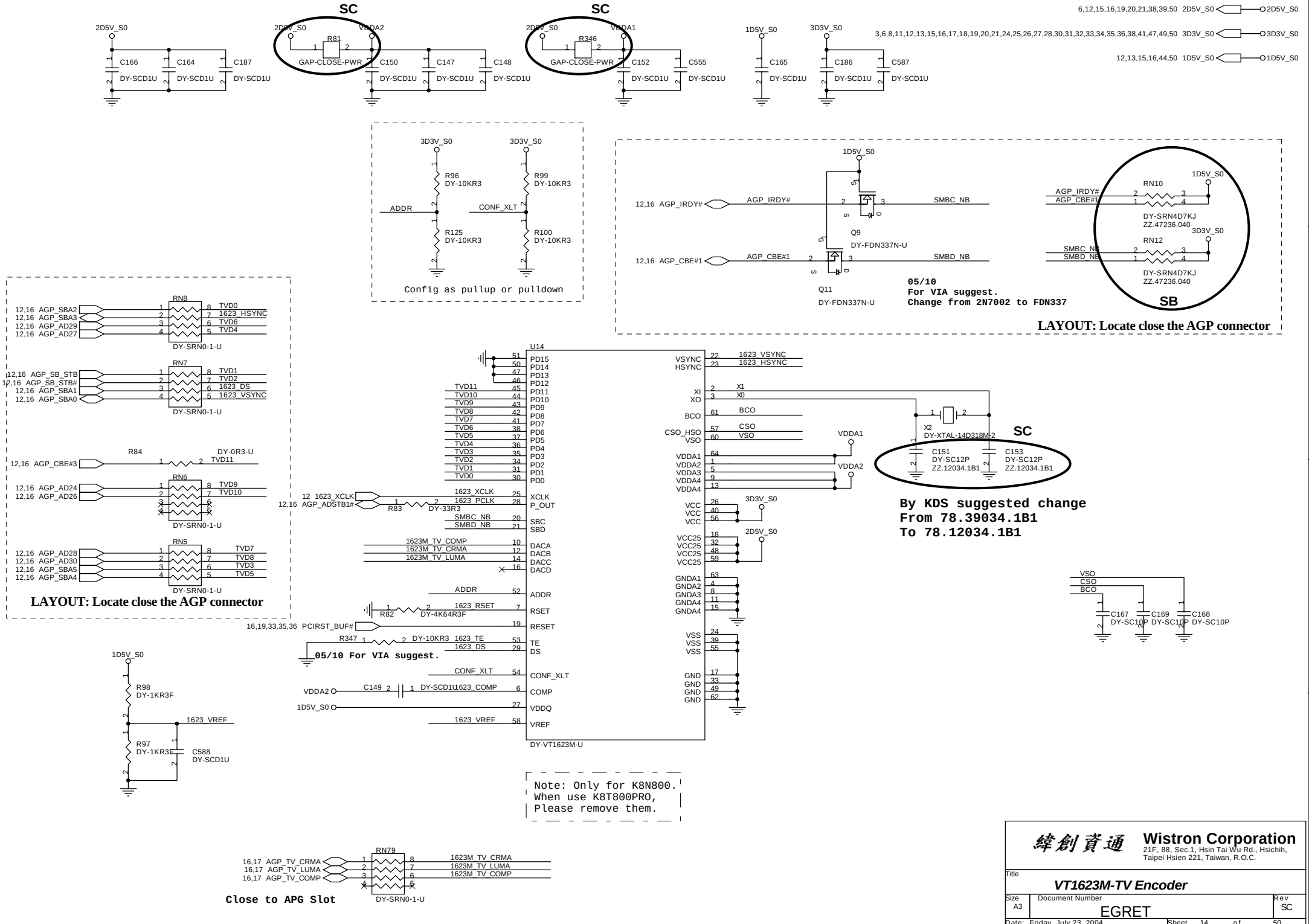


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***NB-K8N800(3/3)_POWER***

Size: A3 | Document Number: **EGRET** | Rev: SC

Date: Friday, July 23, 2004 | Sheet 13 of 50


SC
2D5V_S0
R81
GAP-CLOSE-PWR
VDDA2
C166 DY-SCD1U
C164 DY-SCD1U
C187 DY-SCD1U
C150 DY-SCD1U
C147 DY-SCD1U
C148 DY-SCD1U
R346
VDDA1
C152 DY-SCD1U
C555 DY-SCD1U
1D5V_S0
C165 DY-SCD1U
3D3V_S0
C186 DY-SCD1U
C587 DY-SCD1U
6,12,15,16,19,20,21,38,39,50 2D5V_S0
3,6,8,11,12,13,15,16,17,18,19,20,21,24,25,26,27,28,30,31,32,33,34,35,36,38,41,47,49,50 3D3V_S0
12,13,15,16,44,50 1D5V_S0
R96 DY-10KR3
R99 DY-10KR3
ADDR
CONF_XLT
R125 DY-10KR3
R100 DY-10KR3
Config as pullup or pulldown
12,16 AGP_IRDY#
AGP_IRDY#
SMBC_NB
Q9
DY-FDN337N-U
12,16 AGP_CBE#1
AGP_CBE#1
SMBD_NB
Q11
DY-FDN337N-U
05/10
For VIA suggest.
Change from 2N7002 to FDN337
RN10
DY-SRN4D7KJ
ZZ.47236.040
RN12
SB
LAYOUT: Locate close the AGP connector
RN8
12,16 AGP_SBA2
12,16 AGP_SBA3
12,16 AGP_AD29
12,16 AGP_AD27
TVD0
1623_HSYNC
TVD6
TVD4
DY-SRN0-1-U
RN7
12,16 AGP_SB_STB
12,16 AGP_SB_STB#
12,16 AGP_SBA1
12,16 AGP_SBA0
TVD1
TVD2
1623_DS
1623_VSYNC
R84
DY-0R3-U
12,16 AGP_CBE#3
TVD11
RN6
12,16 AGP_AD24
12,16 AGP_AD26
TVD9
TVD10
RN5
12,16 AGP_AD28
12,16 AGP_AD30
12,16 AGP_SBA5
12,16 AGP_SBA4
TVD7
TVD8
TVD3
TVD5
LAYOUT: Locate close the AGP connector
U14
PD15
PD14
PD13
PD12
PD11
PD10
PD9
PD8
PD7
PD6
PD5
PD4
PD3
PD2
PD1
PD0
VSYNC
HSYNC
1623_VSYNC
1623_HSYNC
XI
XO
X1
X0
BCO
CSO_HSO
VSO
CSO
X2
DY-XTAL-14D318M-2
C151 DY-SC12P ZZ.12034.1B1
C153 DY-SC12P ZZ.12034.1B1
VDDA1
VDDA2
VDDA3
VDDA4
VCC
VCC25
GNDA1
GNDA2
GNDA3
GNDA4
VSS
GND
12 1623_XCLK
12,16 AGP_ADSTB1#
1623_XCLK
1623_PCLK
R83 DY-33R3
XCLK
P_OUT
SMBC_NB
SMBD_NB
SBC
SBD
1623M_TV_COMP
1623M_TV_CRMA
1623M_TV_LUMA
DACA
DACB
DACC
DACD
ADDR
1623_RSET
R82 DY-4K64R3F
RSET
16,19,33,35,36 PCIRST_BUF#
RESET
R347 DY-10KR3
1623_TE
1623_DS
TE
DS
05/10 For VIA suggest.
CONF_XLT
C149 DY-SCD1U
1623_COMP
COMP
VDDQ
1623_VREF
VREF
DY-VT1623M-U
By KDS suggested change
From 78.39034.1B1
To 78.12034.1B1
VSO
CSO
BCO
C167 DY-SC10P
C169 DY-SC10P
C168 DY-SC10P
R98 DY-1KR3F
R97 DY-1KR3F
C588 DY-SCD1U
Note: Only for K8N800.
When use K8T800PRO,
Please remove them.
RN79
16,17 AGP_TV_CRMA
16,17 AGP_TV_LUMA
16,17 AGP_TV_COMP
1623M_TV_CRMA
1623M_TV_LUMA
1623M_TV_COMP
Close to APG Slot
DY-SRN0-1-U
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VT1623M-TV Encoder
Size A3
Document Number
EGRET
Rev SC
Date: Friday, July 23, 2004
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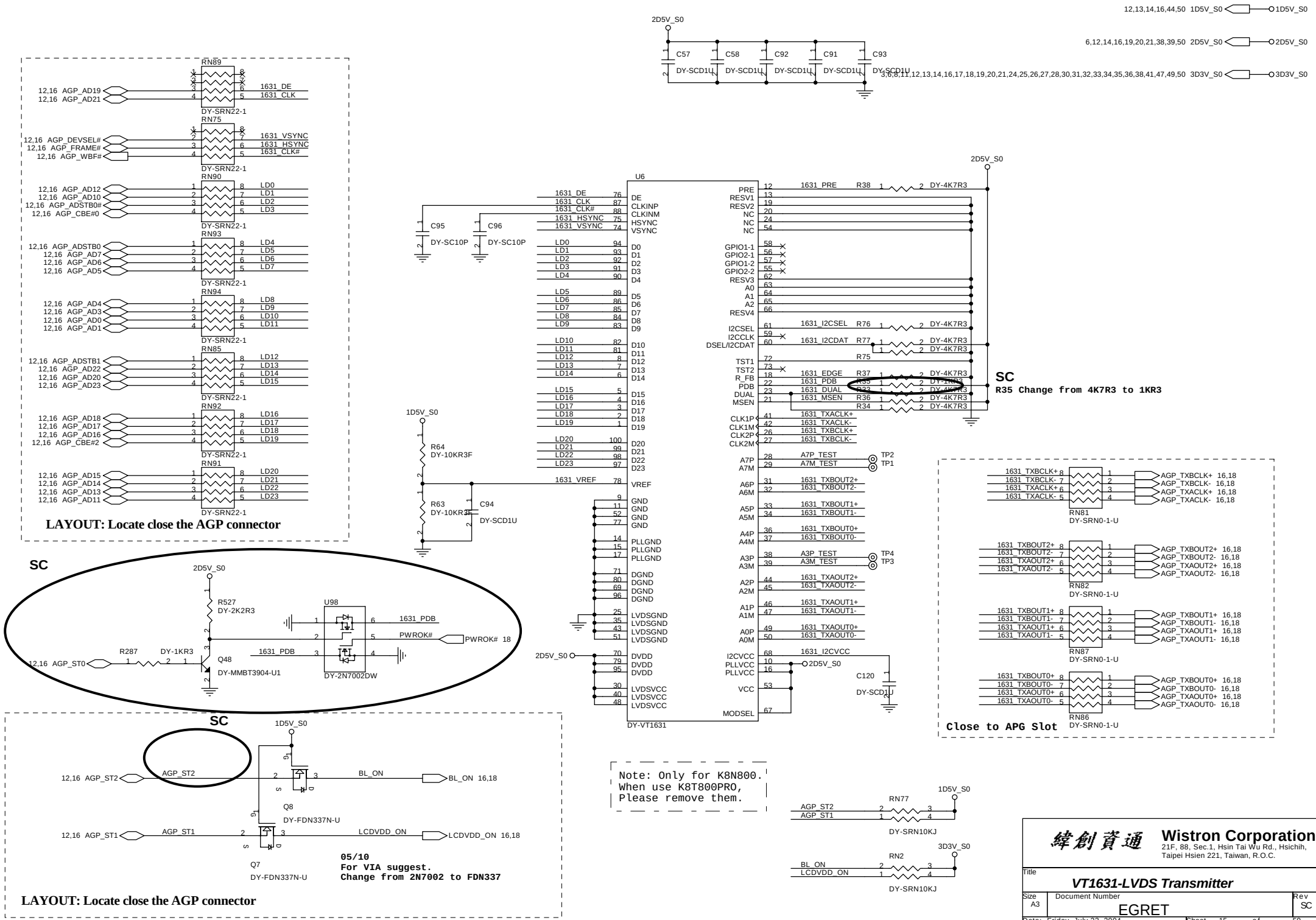
12,13,14,16,44,50 1D5V_S0
6,12,14,16,19,20,21,38,39,50 2D5V_S0
3,6,8,11,12,13,14,16,17,18,19,20,21,24,25,26,27,28,30,31,32,33,34,35,36,38,41,47,49,50 3D3V_S0
2D5V_S0
C57 C58 C92 C91 C93
DY-SCD1U
RN89 RN75 RN90 RN93 RN94 RN85 RN92 RN91
DY-SRN22-1
12,16 AGP_AD19
12,16 AGP_AD21
1631_DE
1631_CLK
12,16 AGP_DEVSEL#
12,16 AGP_FRAME#
12,16 AGP_WBF#
1631_VSYNC
1631_HSYNC
1631_CLK#
12,16 AGP_AD12
12,16 AGP_AD10
12,16 AGP_ADSTB0#
12,16 AGP_CBE#0
LD0 LD1 LD2 LD3
12,16 AGP_ADSTB0
12,16 AGP_AD7
12,16 AGP_AD6
12,16 AGP_AD5
LD4 LD5 LD6 LD7
12,16 AGP_AD4
12,16 AGP_AD3
12,16 AGP_AD0
12,16 AGP_AD1
LD8 LD9 LD10 LD11
12,16 AGP_ADSTB1
12,16 AGP_AD22
12,16 AGP_AD20
12,16 AGP_AD23
LD12 LD13 LD14 LD15
12,16 AGP_AD18
12,16 AGP_AD17
12,16 AGP_AD16
12,16 AGP_CBE#2
LD16 LD17 LD18 LD19
12,16 AGP_AD15
12,16 AGP_AD14
12,16 AGP_AD13
12,16 AGP_AD11
LD20 LD21 LD22 LD23
LAYOUT: Locate close the AGP connector
U6
DY-VT1631
C95 DY-SC10P
C96 DY-SC10P
1631_DE
1631_CLK
1631_CLK#
1631_HSYNC
1631_VSYNC
DE CLKINP CLKINM HSYNC VSYNC
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19 D20 D21 D22 D23
1631_VREF
VREF
GND GND GND GND
PLLGND PLLGND PLLGND
DGND DGND DGND DGND
LVDSGND LVDSGND LVDSGND LVDSGND
DVDD DVDD DVDD
LVDSVCC LVDSVCC LVDSVCC
PRE RESV1 RESV2 NC NC NC
GPIO1-1 GPIO2-1 GPIO1-2 GPIO2-2
RESV3 A0 A1 A2 RESV4
I2CSEL I2CCLK DSEL/I2CDAT
TST1 TST2 R_FB PDB DUAL MSEN
CLK1P CLK1M CLK2P CLK2M
A7P A7M A6P A6M A5P A5M A4P A4M A3P A3M A2P A2M A1P A1M A0P A0M
I2CVCC PLLVCC PLLVCC VCC MODSEL
1631_PRE R38 DY-4K7R3
1631_I2CSEL R76 DY-4K7R3
1631_I2CDAT R77 DY-4K7R3
R75 DY-4K7R3
1631_EDGE R37 DY-4K7R3
1631_PDB R35 DY-1KR3
1631_DUAL R33 DY-4K7R3
1631_MSEN R36 DY-4K7R3
R34 DY-4K7R3
SC
R35 Change from 4K7R3 to 1KR3
1631_TXACLK+
1631_TXACLK-
1631_TXBCLK+
1631_TXBCLK-
A7P_TEST A7M_TEST TP2 TP1
1631_TXBOUT2+ 1631_TXBOUT2-
1631_TXBOUT1+ 1631_TXBOUT1-
1631_TXBOUT0+ 1631_TXBOUT0-
A3P_TEST A3M_TEST TP4 TP3
1631_TXAOUT2+ 1631_TXAOUT2-
1631_TXAOUT1+ 1631_TXAOUT1-
1631_TXAOUT0+ 1631_TXAOUT0-
1631_I2CVCC
2D5V_S0
C120 DY-SCD1U
1D5V_S0
R64 DY-10KR3F
R63 DY-10KR3F
C94 DY-SCD1U
RN81 RN82 RN87 RN86
DY-SRN0-1-U
AGP_TXBCLK+ 16,18
AGP_TXBCLK- 16,18
AGP_TXACLK+ 16,18
AGP_TXACLK- 16,18
AGP_TXBOUT2+ 16,18
AGP_TXBOUT2- 16,18
AGP_TXAOUT2+ 16,18
AGP_TXAOUT2- 16,18
AGP_TXBOUT1+ 16,18
AGP_TXBOUT1- 16,18
AGP_TXAOUT1+ 16,18
AGP_TXAOUT1- 16,18
AGP_TXBOUT0+ 16,18
AGP_TXBOUT0- 16,18
AGP_TXAOUT0+ 16,18
AGP_TXAOUT0- 16,18
Close to APG Slot
SC
2D5V_S0
R527 DY-2K2R3
U98
DY-2N7002DW
1631_PDB
PWROK#
PWROK# 18
R287 DY-1KR3
12,16 AGP_ST0
Q48 DY-MMBT3904-U1
SC
1D5V_S0
12,16 AGP_ST2
AGP_ST2
BL_ON
BL_ON 16,18
Q8 DY-FDN337N-U
12,16 AGP_ST1
AGP_ST1
LCDVDD_ON
LCDVDD_ON 16,18
Q7 DY-FDN337N-U
05/10
For VIA suggest.
Change from 2N7002 to FDN337
LAYOUT: Locate close the AGP connector
Note: Only for K8N800.
When use K8T800PRO,
Please remove them.
RN77 DY-SRN10KJ
AGP_ST2
AGP_ST1
RN2 DY-SRN10KJ
BL_ON
LCDVDD_ON
3D3V_S0
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VT1631-LVDS Transmitter
Size A3
Document Number
EGRET
Rev SC
Date: Friday, July 23, 2004
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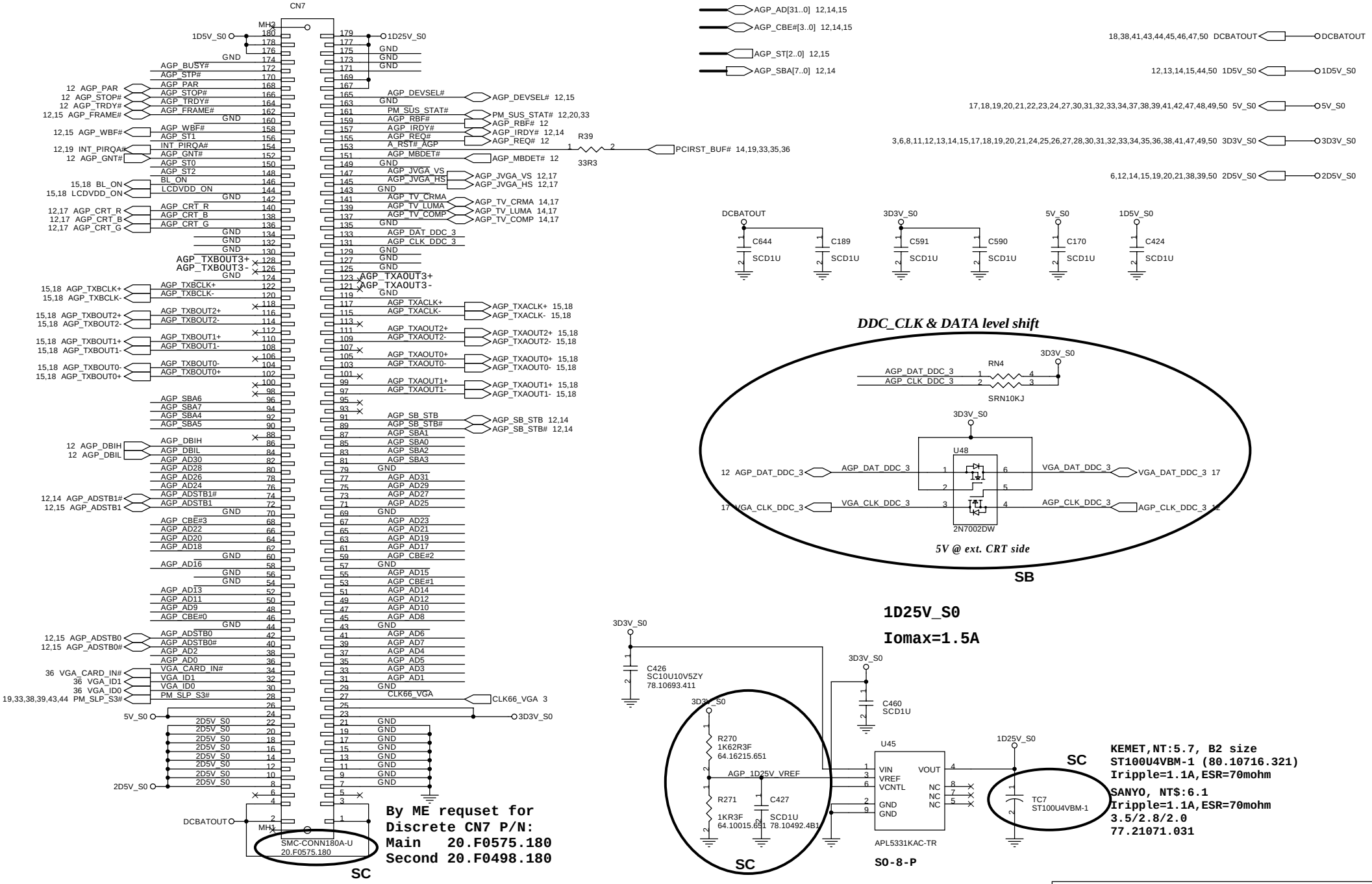
CN7
AGP_AD[31..0] 12,14,15
AGP_CBE#[3..0] 12,14,15
AGP_ST[2..0] 12,15
AGP_SBA[7..0] 12,14
18,38,41,43,44,45,46,47,50 DCBATOUT
12,13,14,15,44,50 1D5V_S0
17,18,19,20,21,22,23,24,27,30,31,32,33,34,37,38,39,41,42,47,48,49,50 5V_S0
3,6,8,11,12,13,14,15,17,18,19,20,21,24,25,26,27,28,30,31,32,33,34,35,36,38,41,47,49,50 3D3V_S0
6,12,14,15,19,20,21,38,39,50 2D5V_S0
DCBATOUT
3D3V_S0
5V_S0
1D5V_S0
C644 SCD1U
C189 SCD1U
C591 SCD1U
C590 SCD1U
C170 SCD1U
C424 SCD1U
DDC_CLK & DATA level shift
RN4
SRN10KJ
U48
2N7002DW
5V @ ext. CRT side
SB
1D25V_S0
Iomax=1.5A
C426 SC10U10V5ZY 78.10693.411
C460 SCD1U
R270 1K62R3F 64.16215.651
R271 1KR3F 64.10015.651
C427 SCD1U 78.10492.4B1
U45
APL5331KAC-TR
SO-8-P
TC7 ST100U4VBM-1
KEMET,NT:5.7, B2 size
ST100U4VBM-1 (80.10716.321)
Iripple=1.1A,ESR=70mohm
SANYO, NT$:6.1
Iripple=1.1A,ESR=70mohm
3.5/2.8/2.0
77.21071.031
SMC-CONN180A-U
20.F0575.180
By ME requset for
Discrete CN7 P/N:
Main 20.F0575.180
Second 20.F0498.180
SC
21 SB_GPI6
R24 DY-0R3-U
20 SB_GPO5
R23 DY-0R3-U
Debug only do not stuff
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Graphic Conn.
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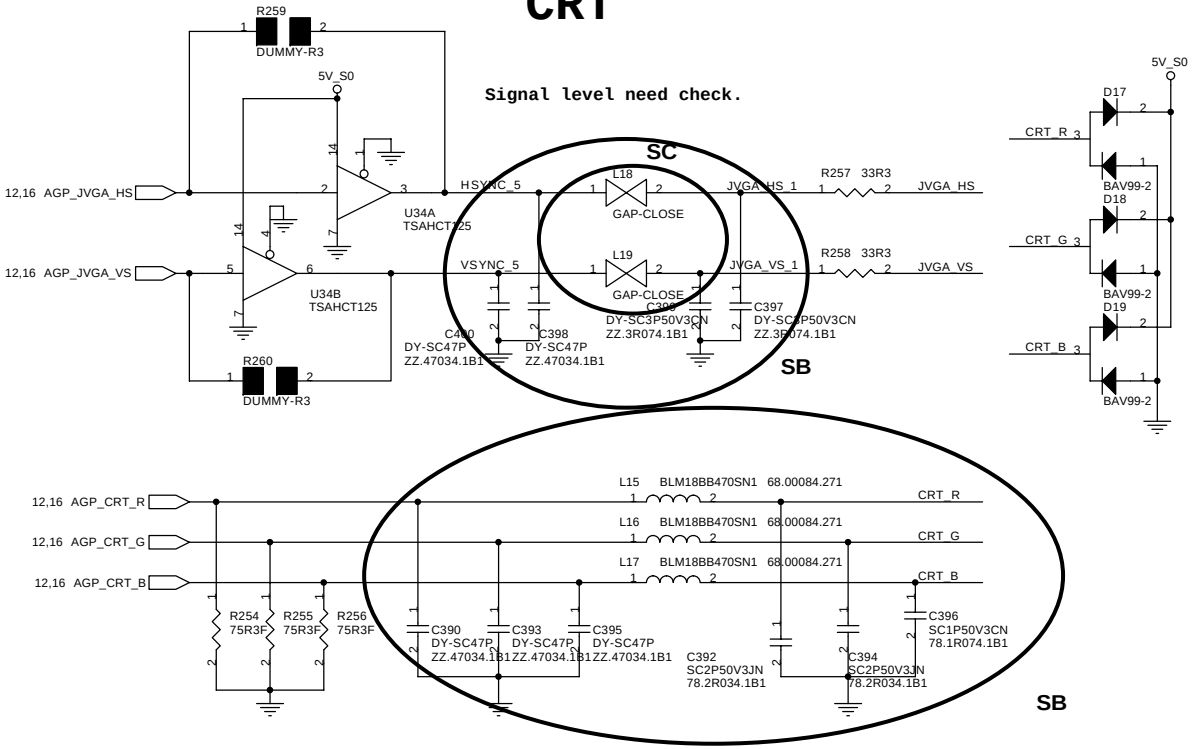
16,18,19,20,21,22,23,24,27,30,31,32,33,34,37,38,39,41,42,47,48,49,50 5V_S0 — 5V_S0

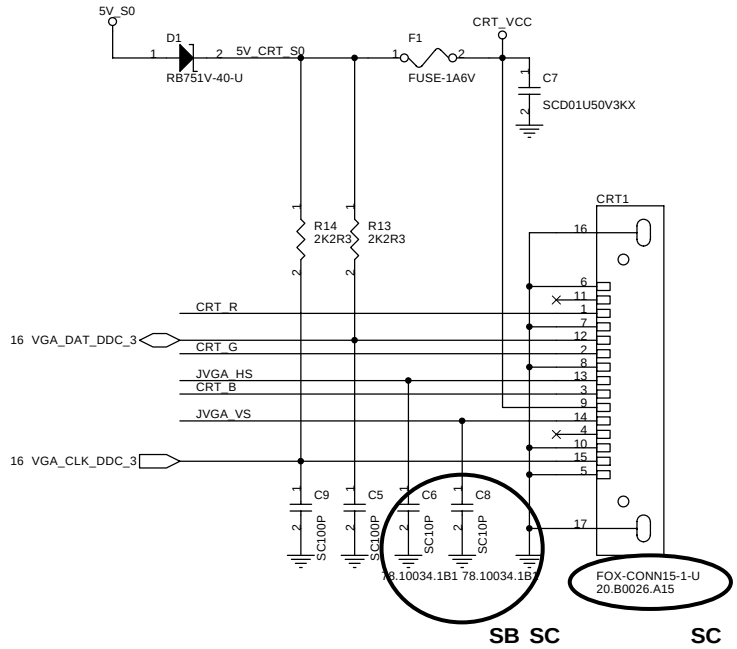
3,6,8,11,12,13,14,15,16,18,19,20,21,24,25,26,27,28,30,31,32,33,34,35,36,38,41,47,49,50 3D3V_S0 — 3D3V_S0

CRT



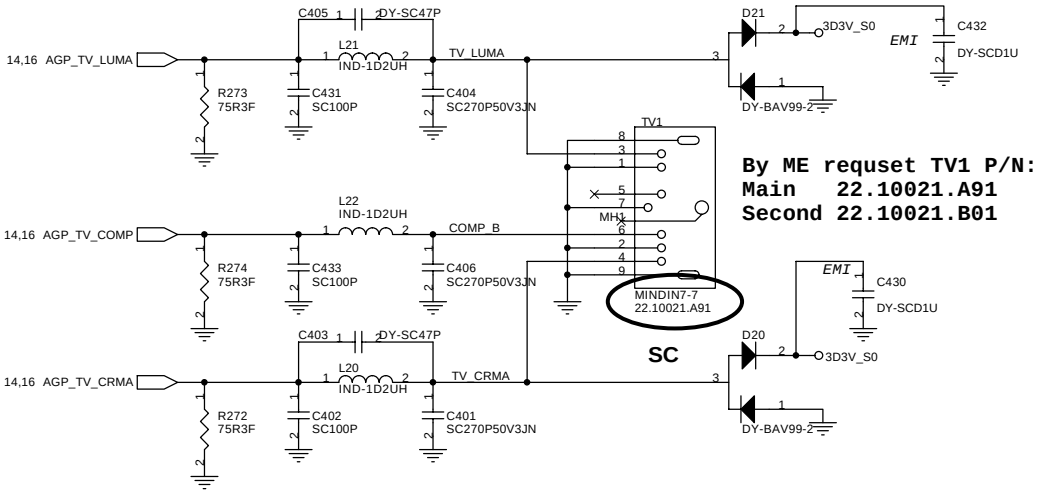
CRT CONN

200mA Rating/Spec 500mA

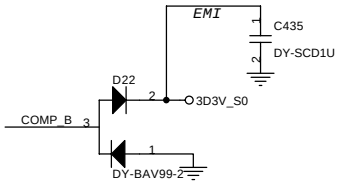


By ME requset CRT1 P/N:
Main 20.B0026.A15
Second 20.B0034.015

TV CONN



By ME requset TV1 P/N:
Main 22.10021.A91
Second 22.10021.B01



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CRT / TV***	
Size A3	Document Number **EGRET**	Rev SC
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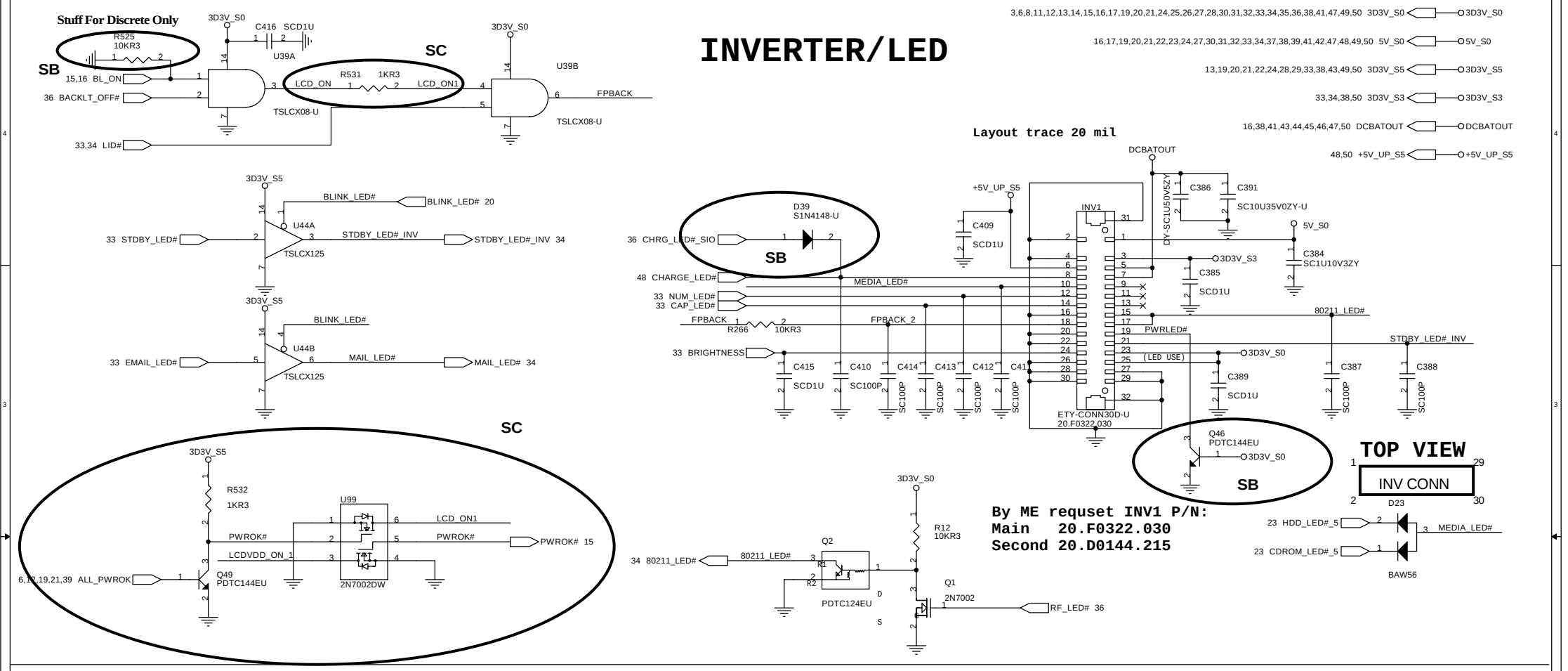
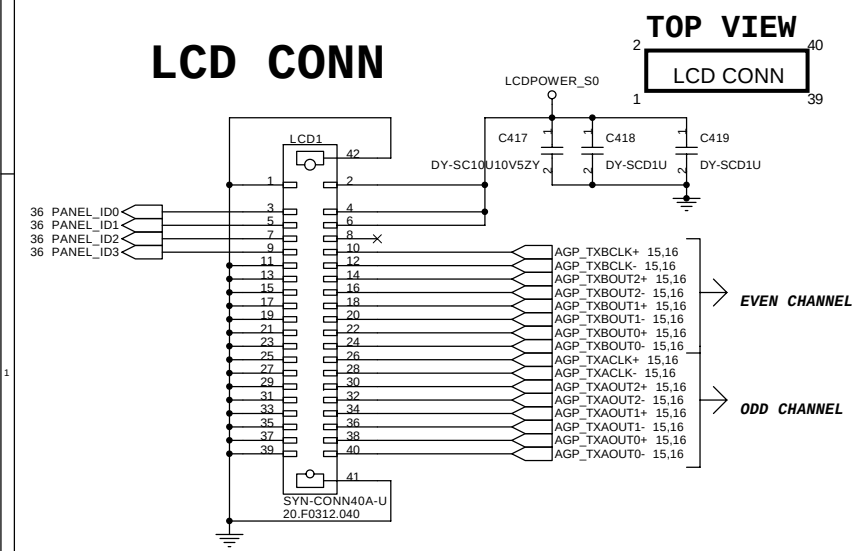
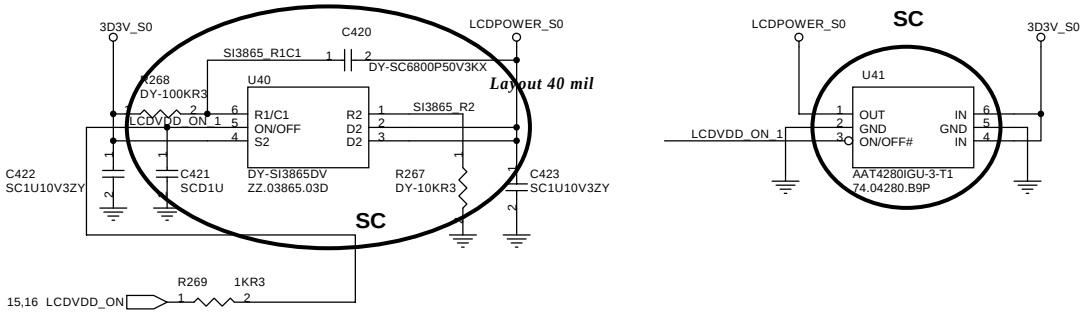
INVERTER/LED



LCD CONN



LCD POWER



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***INV / LCD***	
Size A3	Document Number **EGRET**	Rev SC
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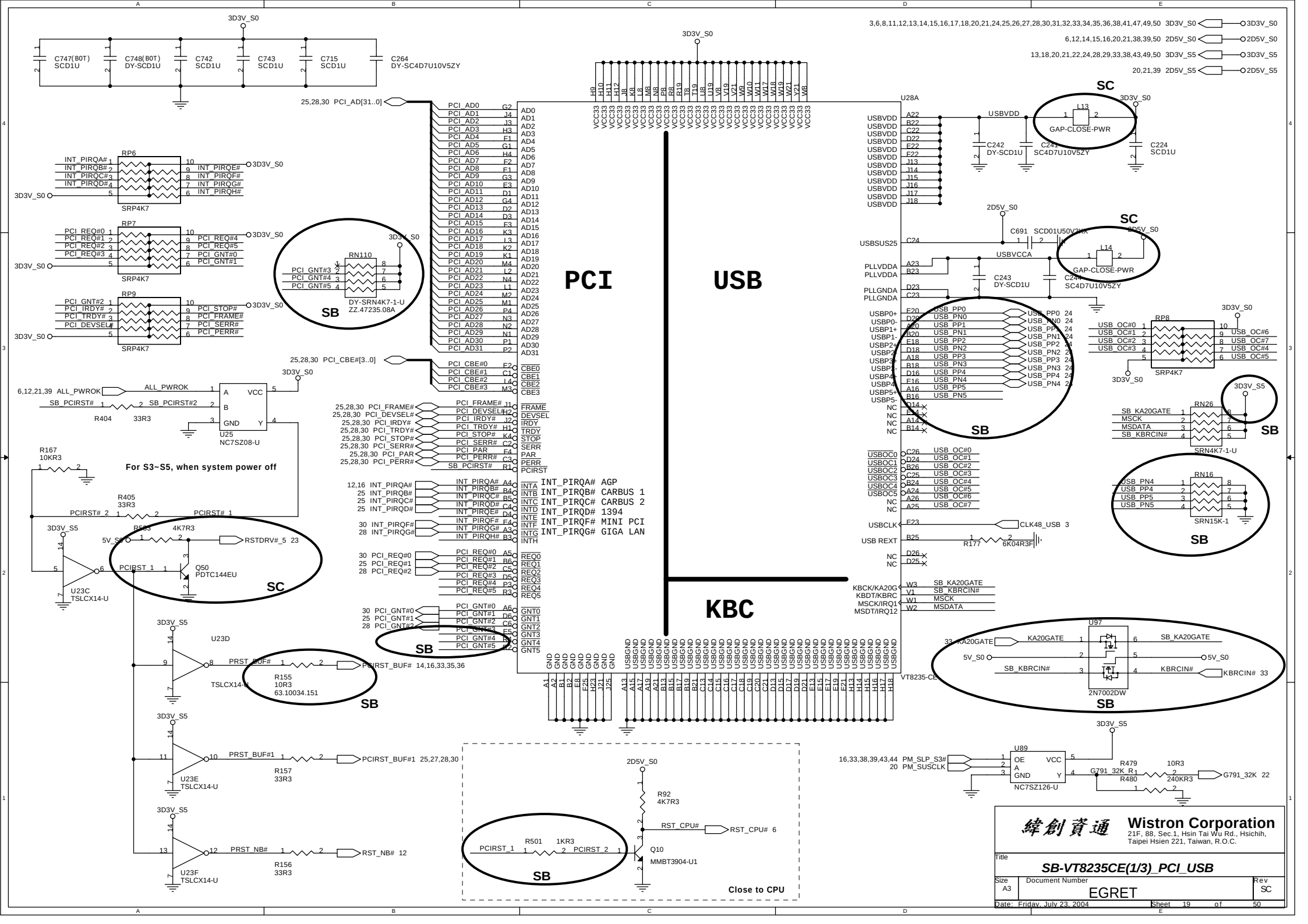
PCI
USB
KBC
U28A
SC
SB
For S3~S5, when system power off
INT_PIRQA# AGP
INT_PIRQB# CARBUS 1
INT_PIRQC# CARBUS 2
INT_PIRQD# 1394
INT_PIRQF# MINI PCI
INT_PIRQG# GIGA LAN
Close to CPU
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
SB-VT8235CE(1/3)_PCI_USB
Size A3
Document Number EGRET
Rev SC
Date: Friday, July 23, 2004
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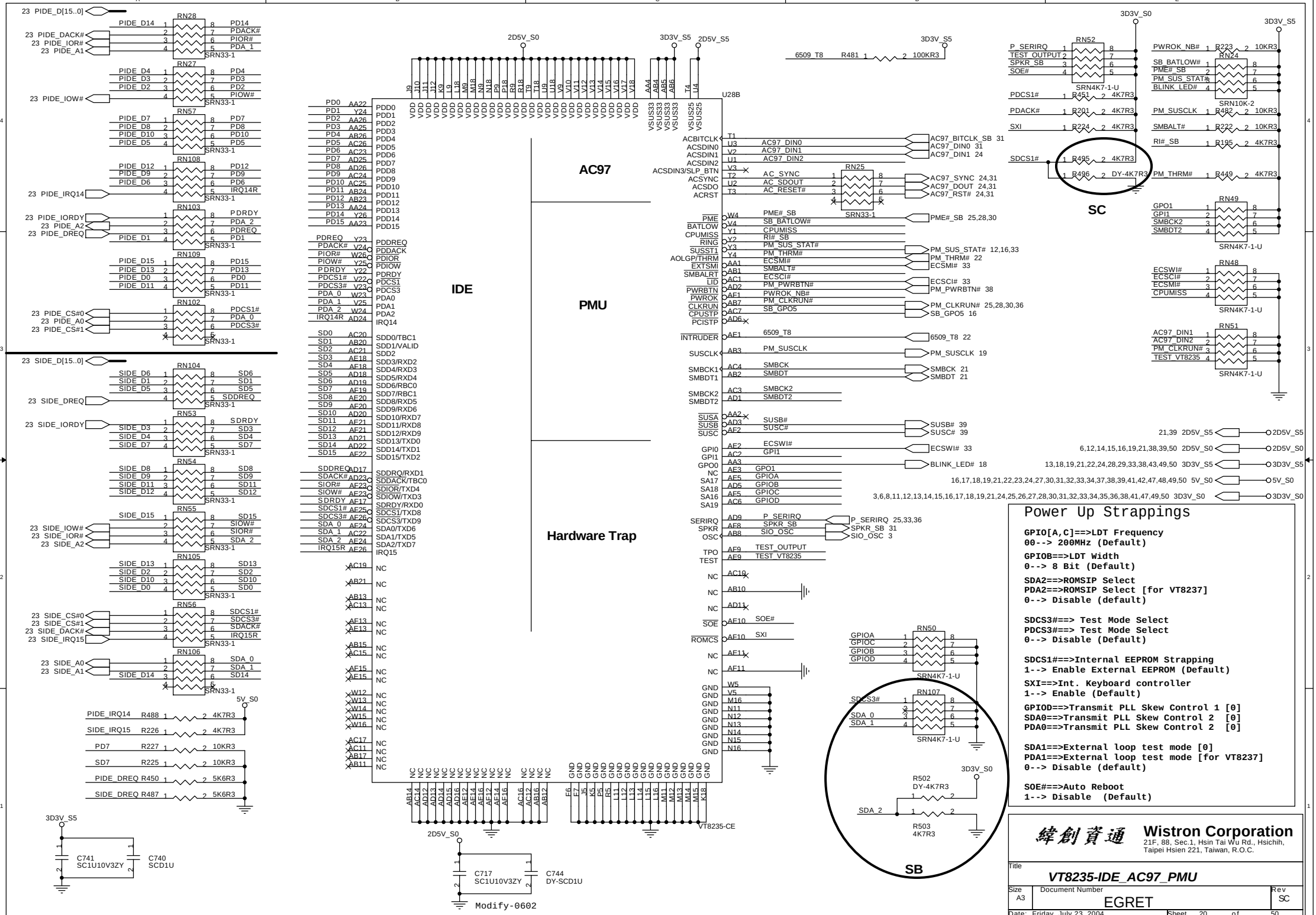
IDE
AC97
PMU
Hardware Trap
U28B
VT8235-CE
SC
SB
Power Up Strappings
GPIO[A,C]==>LDT Frequency
00--> 200MHz (Default)
GPIOB==>LDT Width
0--> 8 Bit (Default)
SDA2==>ROMSIP Select
PDA2==>ROMSIP Select [for VT8237]
0--> Disable (default)
SDCS3#==> Test Mode Select
PDCS3#==> Test Mode Select
0--> Disable (Default)
SDCS1#==>Internal EEPROM Strapping
1--> Enable External EEPROM (Default)
SXI==>Int. Keyboard controller
1--> Enable (Default)
GPIOD==>Transmit PLL Skew Control 1 [0]
SDA0==>Transmit PLL Skew Control 2 [0]
PDA0==>Transmit PLL Skew Control 2 [0]
SDA1==>External loop test mode [0]
PDA1==>External loop test mode [for VT8237]
0--> Disable (default)
SOE#==>Auto Reboot
1--> Disable (Default)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VT8235-IDE_AC97_PMU
Size A3
Document Number
EGRET
Rev SC
Date: Friday, July 23, 2004
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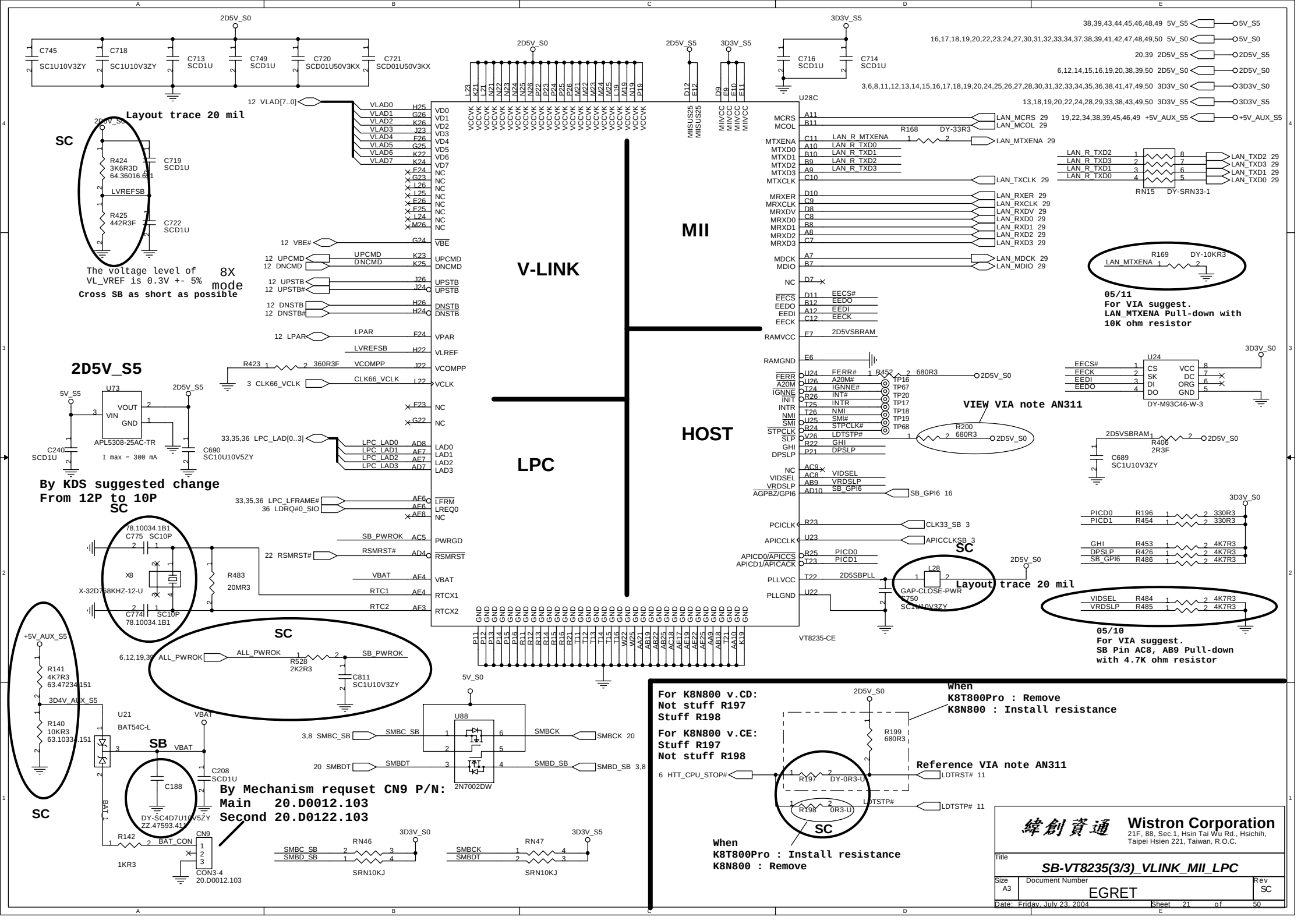
Modify-0602


V-LINK
MII
HOST
LPC
U28C
VT8235-CE
Layout trace 20 mil
SC
The voltage level of VL_VREF is 0.3V +- 5%
Cross SB as short as possible
8X mode
2D5V_S5
By KDS suggested change From 12P to 10P
By Mechanism requset CN9 P/N:
Main 20.D0012.103
Second 20.D0122.103
SB
For K8N800 v.CD:
Not stuff R197
Stuff R198
For K8N800 v.CE:
Stuff R197
Not stuff R198
When K8T800Pro : Remove
K8N800 : Install resistance
Reference VIA note AN311
When K8T800Pro : Install resistance
K8N800 : Remove
05/11
For VIA suggest.
LAN_MTXENA Pull-down with 10K ohm resistor
VIEW VIA note AN311
05/10
For VIA suggest.
SB Pin AC8, AB9 Pull-down with 4.7K ohm resistor
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
SB-VT8235(3/3)_VLINK_MII_LPC
EGRET
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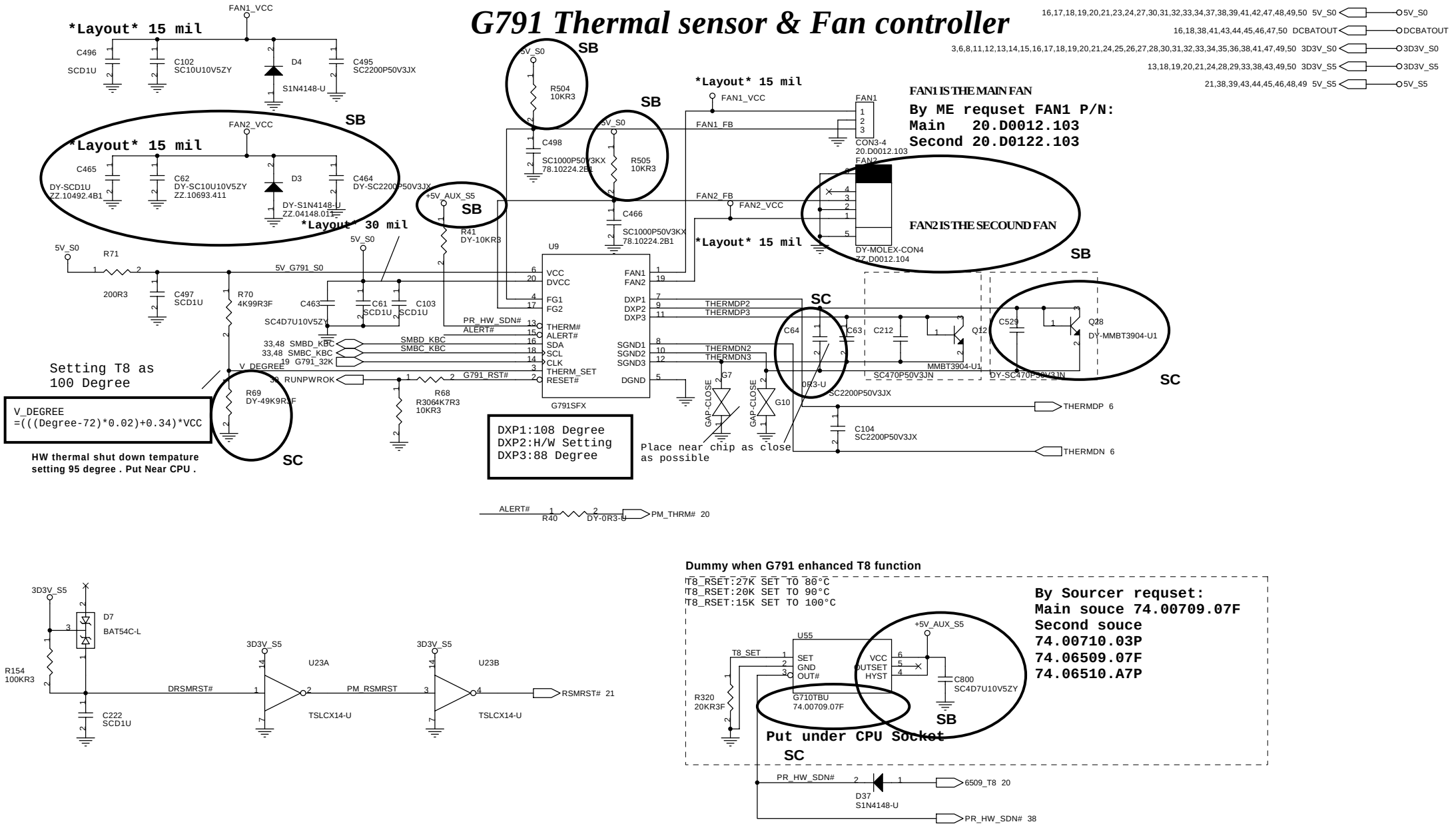
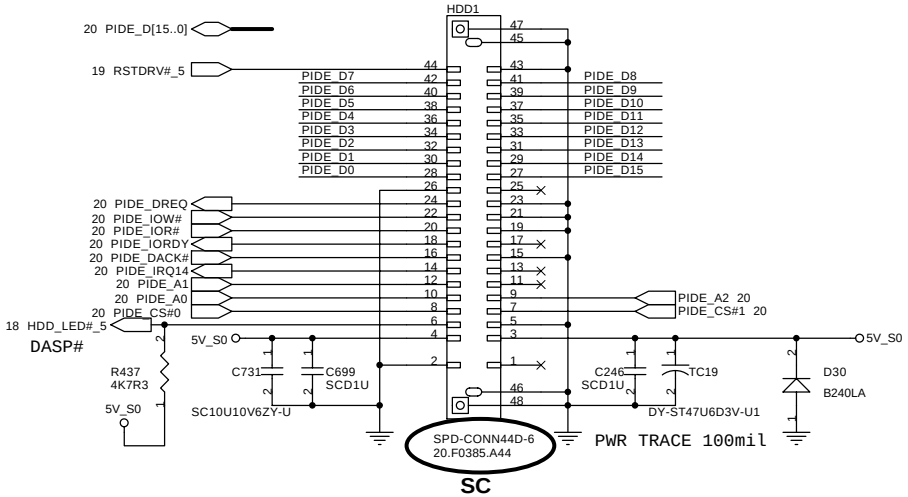
G791 Thermal sensor & Fan controller

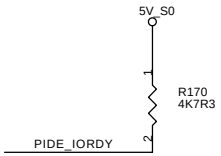


緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***G791***	
Size: Custom	Document Number: EGRET	Rev: SC
Date: Friday, July 23, 2004	Sheet 22 of 50	

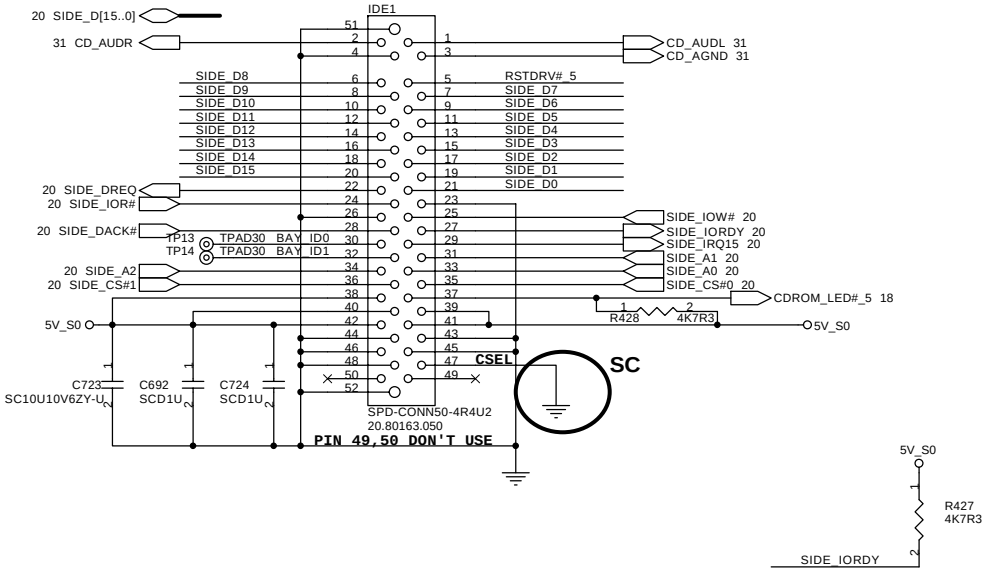
HDD



By ME requset change P/N:
from 20.F0385.044
to 20.F0385.A44



CDROM



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***HDD / CDROM***	
Size A3	Document Number EGRET	Rev SC
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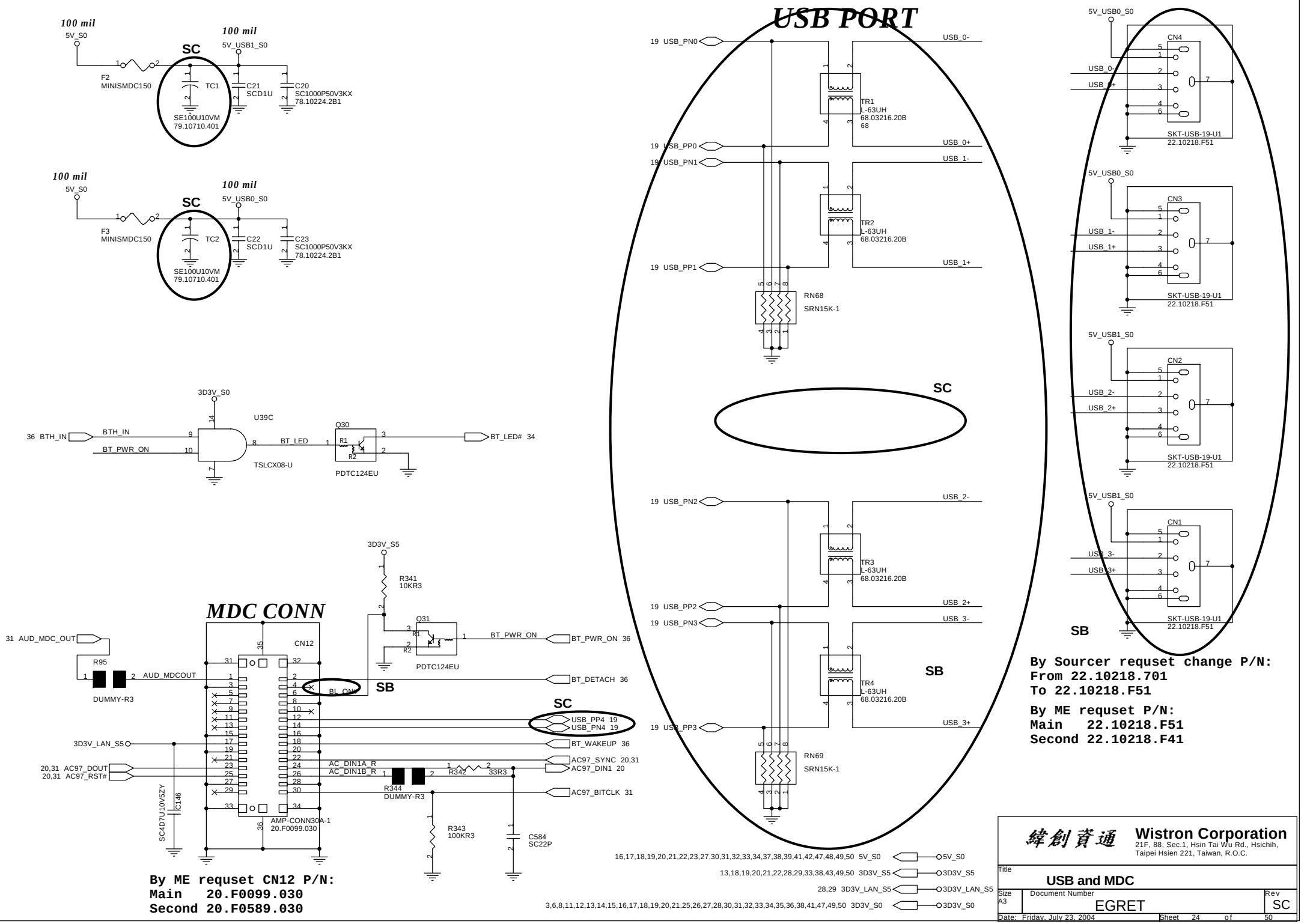
USB PORT
MDC CONN
100 mil
5V_S0
5V_USB1_S0
SC
F2
MINISMDC150
TC1
C21
SCD1U
C20
SC1000P50V3KX
78.10224.2B1
SE100U10VM
79.10710.401
5V_USB0_S0
F3
MINISMDC150
TC2
C22
SCD1U
C23
SC1000P50V3KX
78.10224.2B1
3D3V_S0
U39C
36 BTH_IN
BTH_IN
BT_PWR_ON
BT_LED
TSLCX08-U
Q30
R1
R2
PDTC124EU
BT_LED# 34
3D3V_S5
R341
10KR3
Q31
BT_PWR_ON
BT_PWR_ON 36
31 AUD_MDC_OUT
R95
AUD_MDCOUT
DUMMY-R3
CN12
BT_DETACH 36
SB
BL_ON#
SC
USB_PP4 19
USB_PN4 19
3D3V_LAN_S5
BT_WAKEUP 36
20,31 AC97_DOUT
20,31 AC97_RST#
AC_DIN1A_R
AC_DIN1B_R
R342
33R3
AC97_SYNC 20,31
AC97_DIN1 20
R344
DUMMY-R3
AC97_BITCLK 31
SC4D7U10V5ZY
C146
AMP-CONN30A-1
20.F0099.030
R343
100KR3
C584
SC22P
19 USB_PN0
19 USB_PP0
19 USB_PN1
19 USB_PP1
TR1
L-63UH
68.03216.20B
68
TR2
L-63UH
68.03216.20B
RN68
SRN15K-1
USB_0-
USB_0+
USB_1-
USB_1+
19 USB_PN2
19 USB_PP2
19 USB_PN3
19 USB_PP3
TR3
L-63UH
68.03216.20B
TR4
L-63UH
68.03216.20B
RN69
SRN15K-1
USB_2-
USB_2+
USB_3-
USB_3+
CN4
CN3
CN2
CN1
SKT-USB-19-U1
22.10218.F51
By Sourcer requset change P/N:
From 22.10218.701
To 22.10218.F51
By ME requset P/N:
Main 22.10218.F51
Second 22.10218.F41
By ME requset CN12 P/N:
Main 20.F0099.030
Second 20.F0589.030
16,17,18,19,20,21,22,23,27,30,31,32,33,34,37,38,39,41,42,47,48,49,50 5V_S0
13,18,19,20,21,22,28,29,33,38,43,49,50 3D3V_S5
28,29 3D3V_LAN_S5
3,6,8,11,12,13,14,15,16,17,18,19,20,21,25,26,27,28,30,31,32,33,34,35,36,38,41,47,49,50 3D3V_S0
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
USB and MDC
Size A3
Document Number
EGRET
Rev
SC
Date: Friday, July 23, 2004
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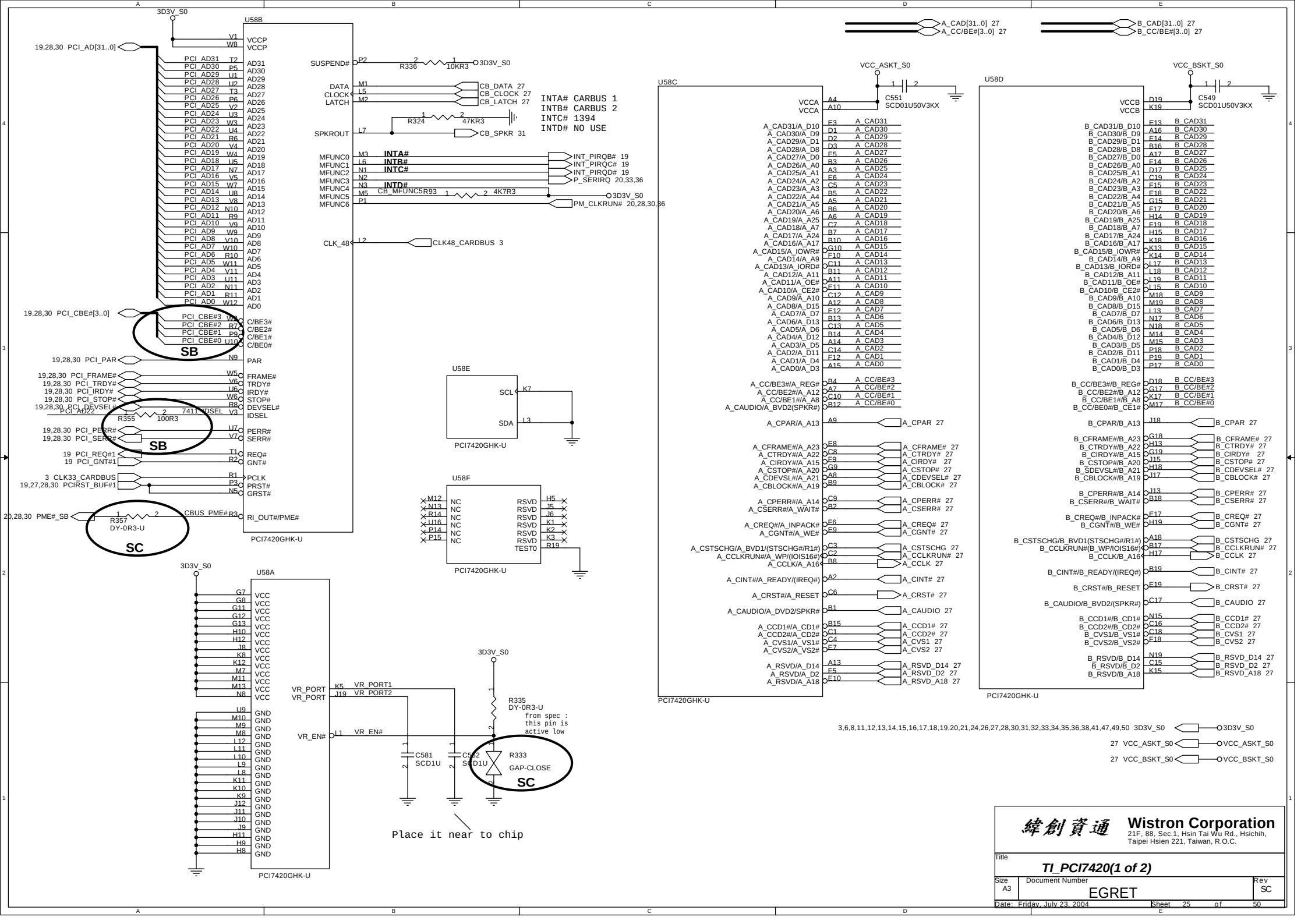
U58B
PCI7420GHK-U
3D3V_S0
19,28,30 PCI_AD[31..0]
19,28,30 PCI_CBE#[3..0]
19,28,30 PCI_PAR
19,28,30 PCI_FRAME#
19,28,30 PCI_TRDY#
19,28,30 PCI_IRDY#
19,28,30 PCI_STOP#
19,28,30 PCI_DEVSEL#
PCI_AD22
R355 100R3
7411 IDSEL
19,28,30 PCI_PERR#
19,28,30 PCI_SERR#
19 PCI_REQ#1
19 PCI_GNT#1
3 CLK33_CARDBUS
19,27,28,30 PCIRST_BUF#1
20,28,30 PME#_SB
R357 DY-0R3-U
CBUS_PME#
SB
SC
SUSPEND#
R336 10KR3
DATA
CLOCK
LATCH
CB_DATA 27
CB_CLOCK 27
CB_LATCH 27
SPKROUT
R324 47KR3
CB_SPKR 31
INTA# CARBUS 1
INTB# CARBUS 2
INTC# 1394
INTD# NO USE
MFUNC0 INTA#
MFUNC1 INTB#
MFUNC2 INTC#
MFUNC3
MFUNC4 INTD#
MFUNC5
MFUNC6
CB_MFUNC5 R93 4K7R3
INT_PIRQB# 19
INT_PIRQC# 19
INT_PIRQD# 19
P_SERIRQ 20,33,36
PM_CLKRUN# 20,28,30,36
CLK_48
CLK48_CARDBUS 3
U58E
SCL
SDA
PCI7420GHK-U
U58F
NC
RSVD
TEST0
U58A
VCC
GND
VR_PORT
VR_PORT1
VR_PORT2
VR_EN#
C581 SCD1U
C582 SCD1U
R335 DY-0R3-U
from spec : this pin is active low
R333 GAP-CLOSE
Place it near to chip
A_CAD[31..0] 27
A_CC/BE#[3..0] 27
B_CAD[31..0] 27
B_CC/BE#[3..0] 27
VCC_ASKT_S0
C551 SCD01U50V3KX
U58C
VCCA
A_CAD31/A_D10
A_CAD30/A_D9
A_CAD29/A_D1
A_CAD28/A_D8
A_CAD27/A_D0
A_CAD26/A_A0
A_CAD25/A_A1
A_CAD24/A_A2
A_CAD23/A_A3
A_CAD22/A_A4
A_CAD21/A_A5
A_CAD20/A_A6
A_CAD19/A_A25
A_CAD18/A_A7
A_CAD17/A_A24
A_CAD16/A_A17
A_CAD15/A_IOWR#
A_CAD14/A_A9
A_CAD13/A_IORD#
A_CAD12/A_A11
A_CAD11/A_OE#
A_CAD10/A_CE2#
A_CAD9/A_A10
A_CAD8/A_D15
A_CAD7/A_D7
A_CAD6/A_D13
A_CAD5/A_D6
A_CAD4/A_D12
A_CAD3/A_D5
A_CAD2/A_D11
A_CAD1/A_D4
A_CAD0/A_D3
A_CC/BE3#/A_REG#
A_CC/BE2#/A_A12
A_CC/BE1#/A_A8
A_CAUDIO/A_BVD2(SPKR#)
A_CPAR/A_A13
A_CFRAME#/A_A23
A_CTRDY#/A_A22
A_CIRDY#/A_A15
A_CSTOP#/A_A20
A_CDEVSL#/A_A21
A_CBLOCK#/A_A19
A_CPERR#/A_A14
A_CSERR#/A_WAIT#
A_CREQ#/A_INPACK#
A_CGNT#/A_WE#
A_CSTSCHG/A_BVD1/(STSCHG#/R1#)
A_CCLKRUN#/A_WP/(IOIS16#)
A_CCLK/A_A16
A_CINT#/A_READY/(IREQ#)
A_CRST#/A_RESET
A_CAUDIO/A_DVD2/SPKR#
A_CCD1#/A_CD1#
A_CCD2#/A_CD2#
A_CVS1/A_VS1#
A_CVS2/A_VS2#
A_RSVD/A_D14
A_RSVD/A_D2
A_RSVD/A_A18
VCC_BSKT_S0
C549 SCD01U50V3KX
U58D
VCCB
B_CAD31/B_D10
B_CAD30/B_D9
B_CAD29/B_D1
B_CAD28/B_D8
B_CAD27/B_D0
B_CAD26/B_A0
B_CAD25/B_A1
B_CAD24/B_A2
B_CAD23/B_A3
B_CAD22/B_A4
B_CAD21/B_A5
B_CAD20/B_A6
B_CAD19/B_A25
B_CAD18/B_A7
B_CAD17/B_A24
B_CAD16/B_A17
B_CAD15/B_IOWR#
B_CAD14/B_A9
B_CAD13/B_IORD#
B_CAD12/B_A11
B_CAD11/B_OE#
B_CAD10/B_CE2#
B_CAD9/B_A10
B_CAD8/B_D15
B_CAD7/B_D7
B_CAD6/B_D13
B_CAD5/B_D6
B_CAD4/B_D12
B_CAD3/B_D5
B_CAD2/B_D11
B_CAD1/B_D4
B_CAD0/B_D3
B_CC/BE3#/B_REG#
B_CC/BE2#/B_A12
B_CC/BE1#/B_A8
B_CC/BE0#/B_CE1#
B_CPAR/B_A13
B_CFRAME#/B_A23
B_CTRDY#/B_A22
B_CIRDY#/B_A15
B_CSTOP#/B_A20
B_SDEVSL#/B_A21
B_CBLOCK#/B_A19
B_CPERR#/B_A14
B_CSERR#/B_WAIT#
B_CREQ#/B_INPACK#
B_CGNT#/B_WE#
B_CSTSCHG/B_BVD1(STSCHG#/R1#)
B_CCLKRUN#(B_WP/IOIS16#)
B_CCLK/B_A16
B_CINT#/B_READY/(IREQ#)
B_CRST#/B_RESET
B_CAUDIO/B_BVD2/(SPKR#)
B_CCD1#/B_CD1#
B_CCD2#/B_CD2#
B_CVS1/B_VS1#
B_CVS2/B_VS2#
B_RSVD/B_D14
B_RSVD/B_D2
B_RSVD/B_A18
3,6,8,11,12,13,14,15,16,17,18,19,20,21,24,26,27,28,30,31,32,33,34,35,36,38,41,47,49,50 3D3V_S0
27 VCC_ASKT_S0
27 VCC_BSKT_S0
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
TI_PCI7420(1 of 2)
Size A3
Document Number
EGRET
Rev SC
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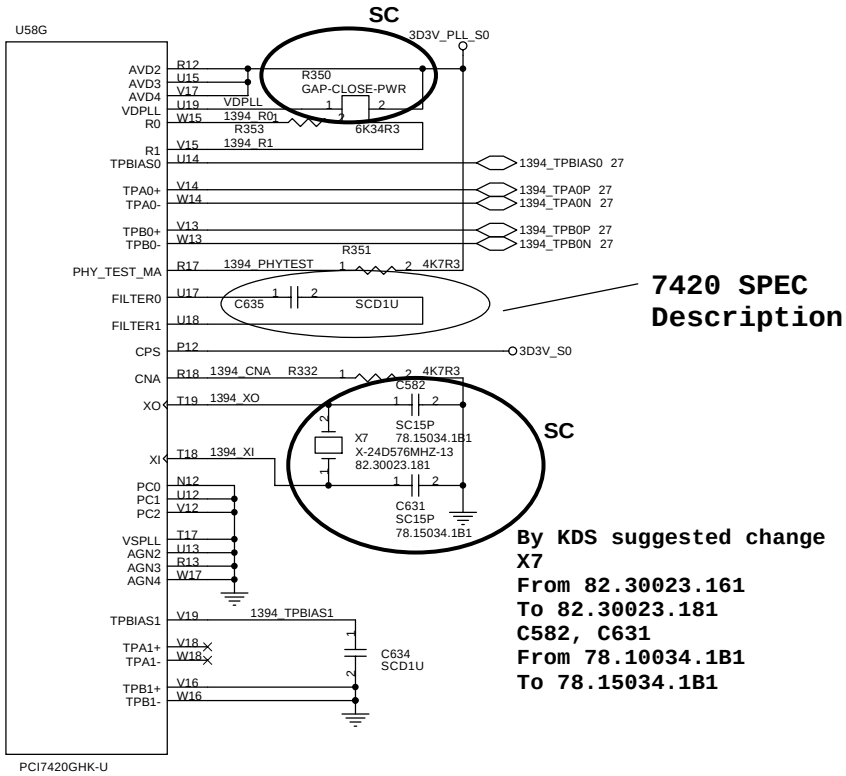
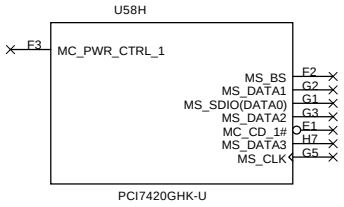
3,6,8,11,12,13,14,15,16,17,18,19,20,21,24,25,27,28,30,31,32,33,34,35,36,38,41,47,49,50 3D3V_S0 3D3V_S0

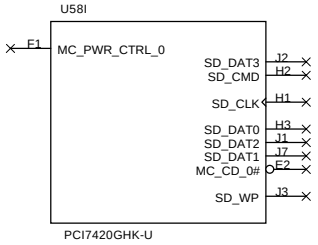


7420 SPEC Description

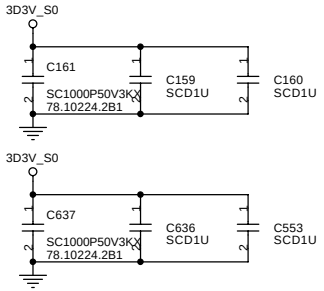
SC

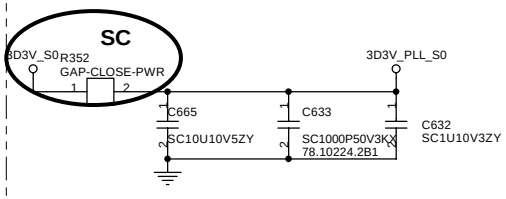
By KDS suggested change
X7
From 82.30023.161
To 82.30023.181
C582, C631
From 78.10034.1B1
To 78.15034.1B1





Bypass/Decupoling Capacitors
Should be places as close to
PCI7420 as possible





緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***TI_PCI7420(2 of 2)***	
Size A3	Document Number EGRET	Rev SC
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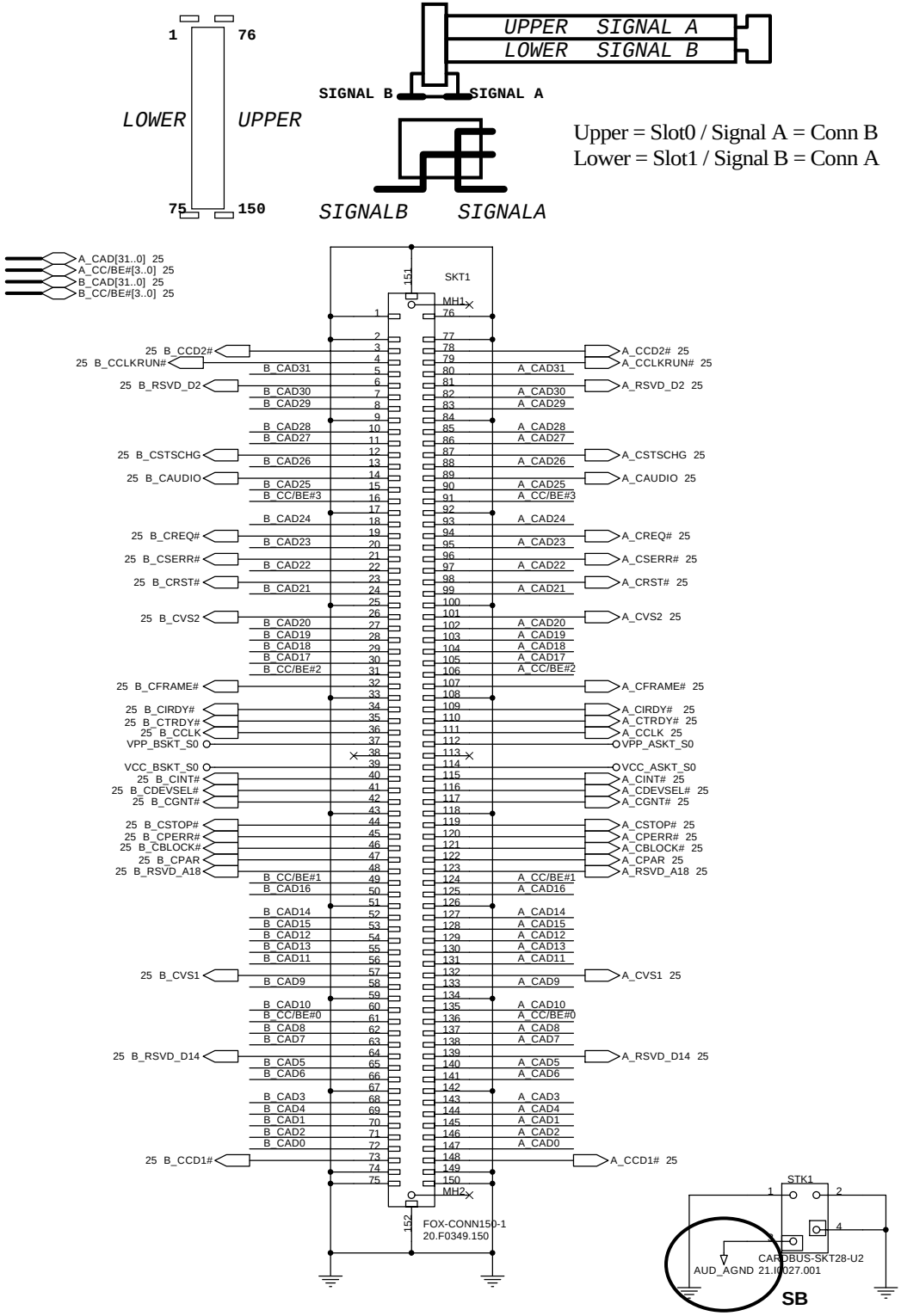
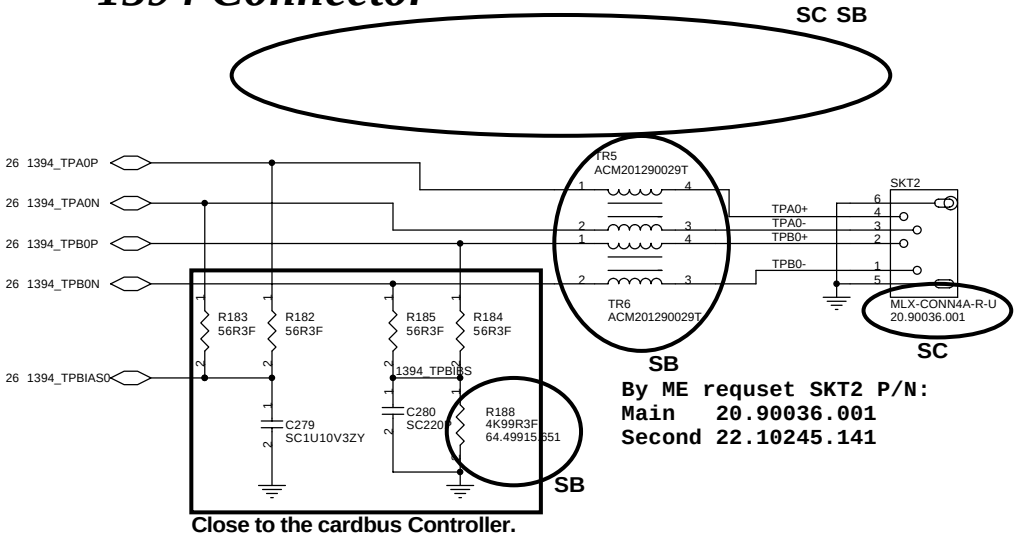


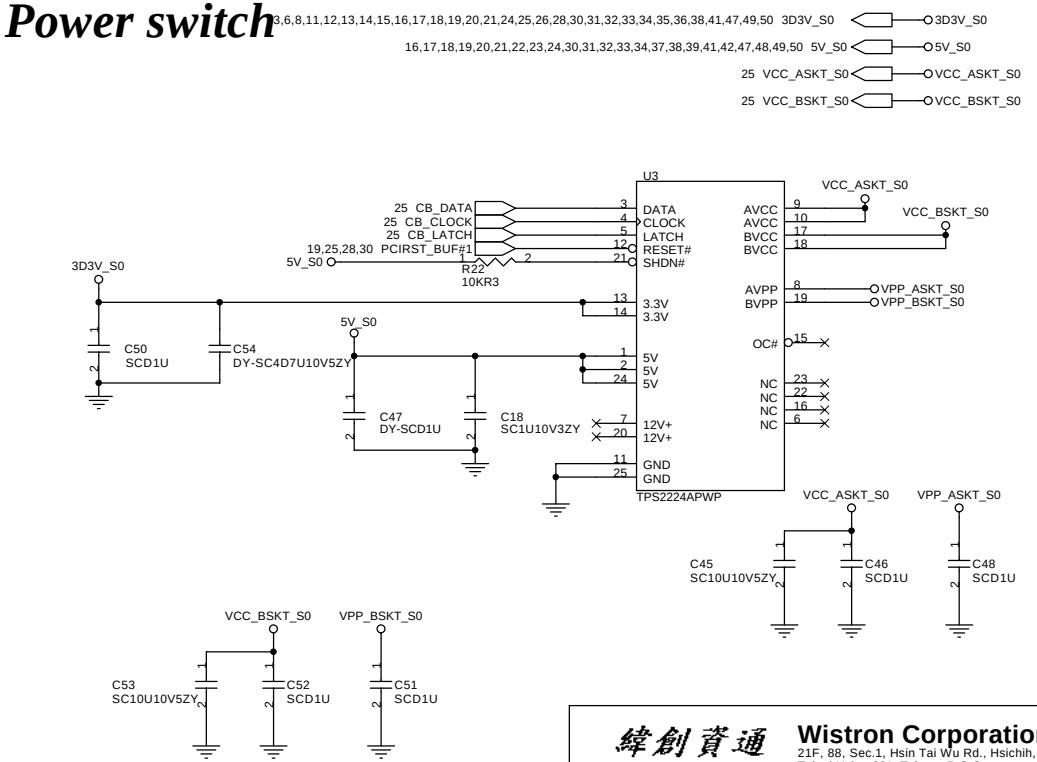
1394 Connector

**

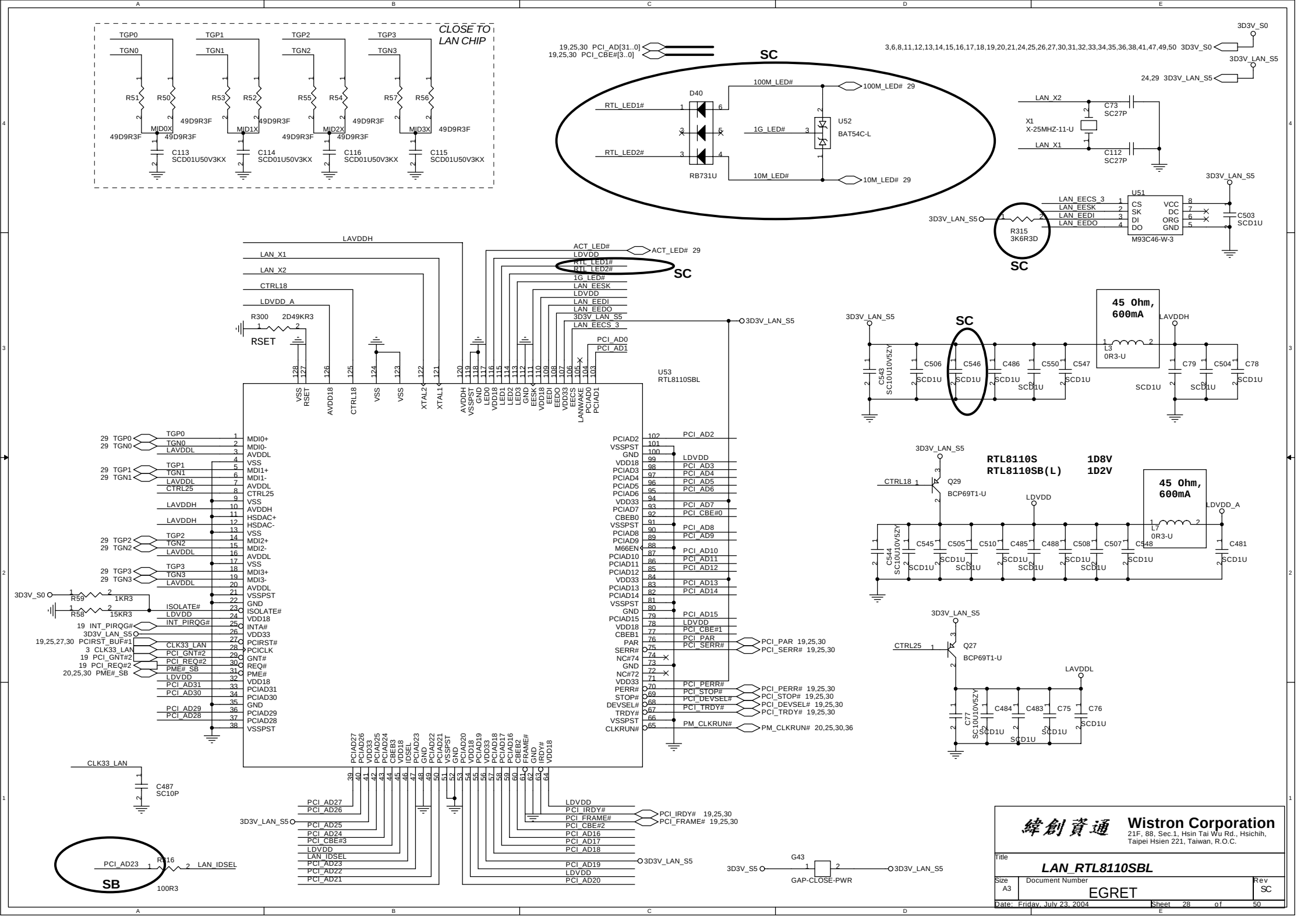


By ME requset SKT2 P/N:
Main 20.90036.001
Second 22.10245.141

Power switch



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***PCMCA SLOT_1394 CONN***
Size A3	Document Number EGRET — Rev SC
Date: Friday, July 23, 2004	Sheet 27 of 50


CLOSE TO LAN CHIP
TGP0 TGN0 TGP1 TGN1 TGP2 TGN2 TGP3 TGN3
R51 R50 R53 R52 R55 R54 R57 R56
49D9R3F
MID0X MID1X MID2X MID3X
C113 SCD01U50V3KX
C114 SCD01U50V3KX
C116 SCD01U50V3KX
C115 SCD01U50V3KX
SC
D40
RB731U
RTL_LED1#
RTL_LED2#
100M_LED#
1G_LED#
10M_LED#
U52
BAT54C-L
19,25,30 PCI_AD[31..0]
19,25,30 PCI_CBE#[3..0]
3,6,8,11,12,13,14,15,16,17,18,19,20,21,24,25,26,27,30,31,32,33,34,35,36,38,41,47,49,50 3D3V_S0
3D3V_S0
3D3V_LAN_S5
24,29 3D3V_LAN_S5
LAN_X2
LAN_X1
X1
X-25MHZ-11-U
C73 SC27P
C112 SC27P
U51
M93C46-W-3
LAN_EECS_3
LAN_EESK
LAN_EEDI
LAN_EEDO
R315 3K6R3D
C503 SCD1U
LAVDDH
LDVDD_A
R300 2D49KR3
RSET
ACT_LED#
LDVDD
LAN_EEDO
3D3V_LAN_S5
PCI_AD0
PCI_AD1
U53
RTL8110SBL
45 Ohm, 600mA
L3 0R3-U
C543 SC10U10V5Y
C506 SCD1U
C546 SCD1U
C486 SCD1U
C550 SCD1U
C547 SCD1U
C79 SCD1U
C504 SCD1U
C78 SCD1U
RTL8110S 1D8V
RTL8110SB(L) 1D2V
Q29 BCP69T1-U
L7 0R3-U
C544 SC10U10V5Y
C545 SCD1U
C505 SCD1U
C510 SCD1U
C485 SCD1U
C488 SCD1U
C508 SCD1U
C507 SCD1U
C548 SCD1U
C481 SCD1U
Q27 BCP69T1-U
C77 SC10U10V5Y
C484 SCD1U
C483 SCD1U
C75 SCD1U
C76 SCD1U
MDI0+ MDI0- MDI1+ MDI1- MDI2- MDI2+ MDI3+ MDI3-
CTRL25 HSDAC+ HSDAC-
ISOLATE# INT_PIRQG# INTA# PCIRST# PCICLK GNT# REQ# PME#
CLK33_LAN PCI_GNT#2 PCI_REQ#2 PME#_SB
PCI_AD31 PCI_AD30 PCI_AD29 PCI_AD28
PCIAD2 PCIAD3 PCIAD4 PCIAD5 PCIAD6 PCIAD7 CBEB0 PCIAD8 PCIAD9 M66EN PCIAD10 PCIAD11 PCIAD12 PCIAD13 PCIAD14 PCIAD15 CBEB1 PAR SERR# NC#74 NC#72 PERR# STOP# DEVSEL# TRDY# CLKRUN#
PCI_AD2 PCI_AD3 PCI_AD4 PCI_AD5 PCI_AD6 PCI_AD7 PCI_CBE#0 PCI_AD8 PCI_AD9 PCI_AD10 PCI_AD11 PCI_AD12 PCI_AD13 PCI_AD14 PCI_AD15 PCI_CBE#1 PCI_PAR PCI_SERR# PCI_PERR# PCI_STOP# PCI_DEVSEL# PCI_TRDY# PM_CLKRUN#
PCI_PAR 19,25,30
PCI_SERR# 19,25,30
PCI_PERR# 19,25,30
PCI_STOP# 19,25,30
PCI_DEVSEL# 19,25,30
PCI_TRDY# 19,25,30
PM_CLKRUN# 20,25,30,36
PCI_IRDY# 19,25,30
PCI_FRAME# 19,25,30
CLK33_LAN
C487 SC10P
PCI_AD23 R316 100R3 LAN_IDSEL
SB
G43 GAP-CLOSE-PWR
3D3V_S5
3D3V_LAN_S5
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
LAN_RTL8110SBL
Size A3
Document Number EGRET
Rev SC
Date: Friday, July 23, 2004
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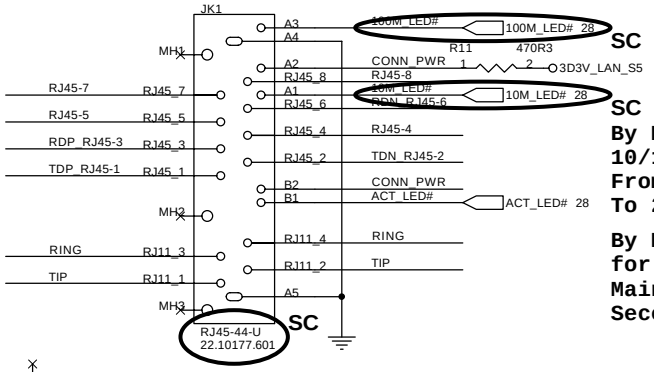
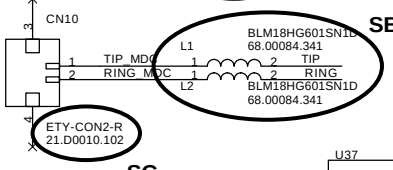
Link: Green - 10Mbps/802.11b
Orange - 100Mbps/802.11a
Yellow - 1Gbps

Activity: Yellow

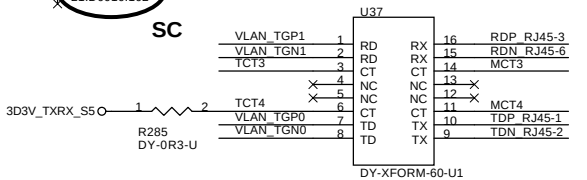


By ME requset for
10/100 LAN change P/N:
From 22.10177.601
To 22.10177.621

By ME requset
for GigaLAN JK1 P/N:
Main 22.10177.601
Second 22.10245.771

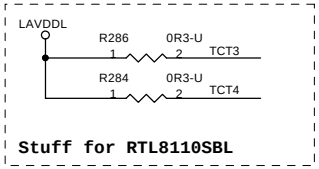


By ME requset change P/N:
From 20.D0121.102
To 21.D0010.102



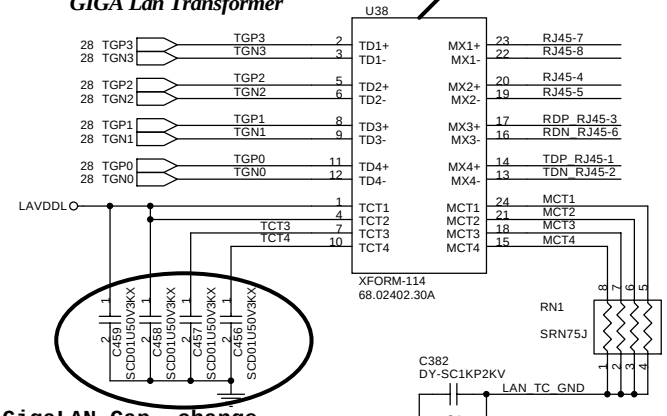
Stuff for VT6103L
10/100M Lan Transformer

By Sourcer requset change P/N:
From 68.H0013.301
To 68.0H80P.301

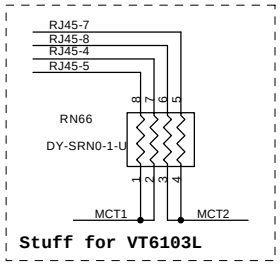


By Sourcer requset change P/N:
From 68.H5015.301
To 68.02402.30A

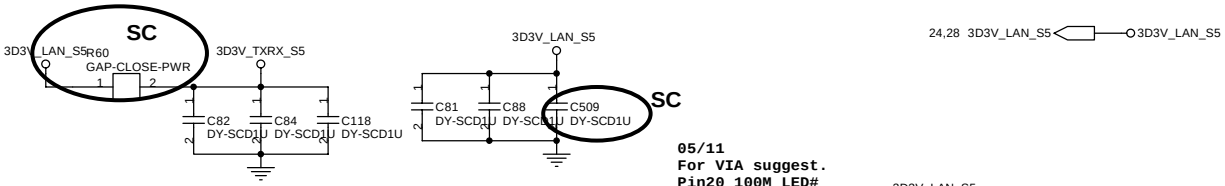
GIGA Lan Transformer



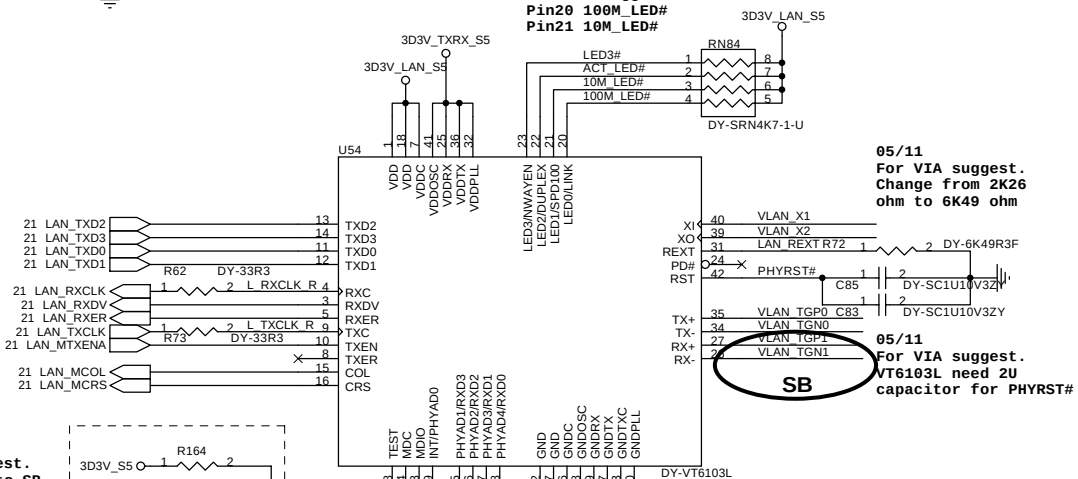
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.



For GigaLAN Cap. change
to SCD01U50V3KX
78.10324.2B1



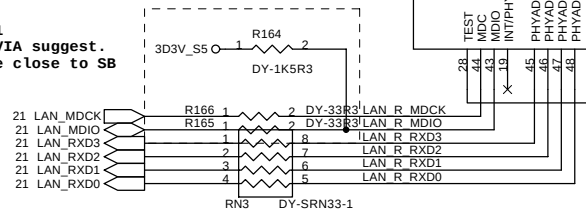
05/11
For VIA suggest.
Pin20 100M_LED#
Pin21 10M_LED#

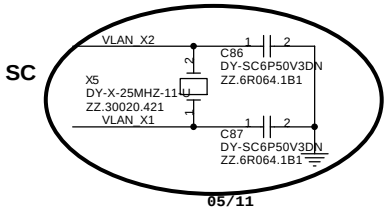


05/11
For VIA suggest.
Change from 2K26
ohm to 6K49 ohm

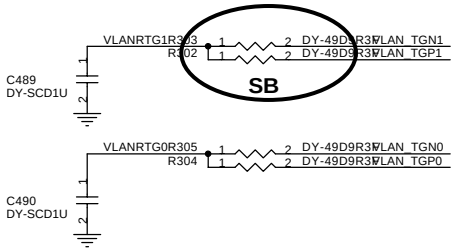
05/11
For VIA suggest.
VT6103L need 2U
capacitor for PHYRST#

05/11
For VIA suggest.
Place close to SB





05/11
For VIA suggest.
Change from 18P to 22P



By KDS suggested change
X5
From 82.30020.161
To 82.30023.421
C86, C87
From 22P To 6P

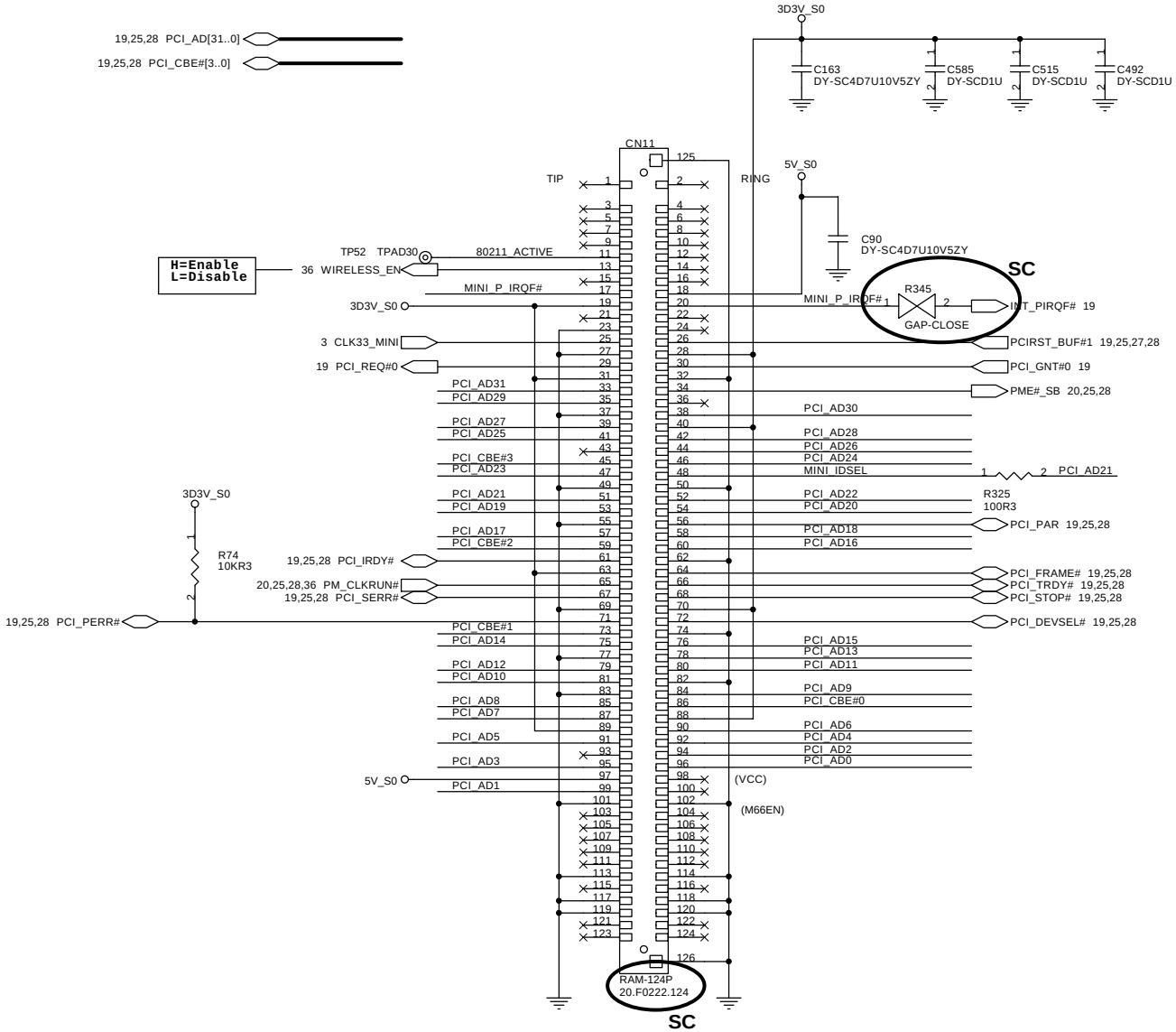
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LAN_CONN&10/100LAN*

Size: A3 | Document Number: EGRET | Rev: SC

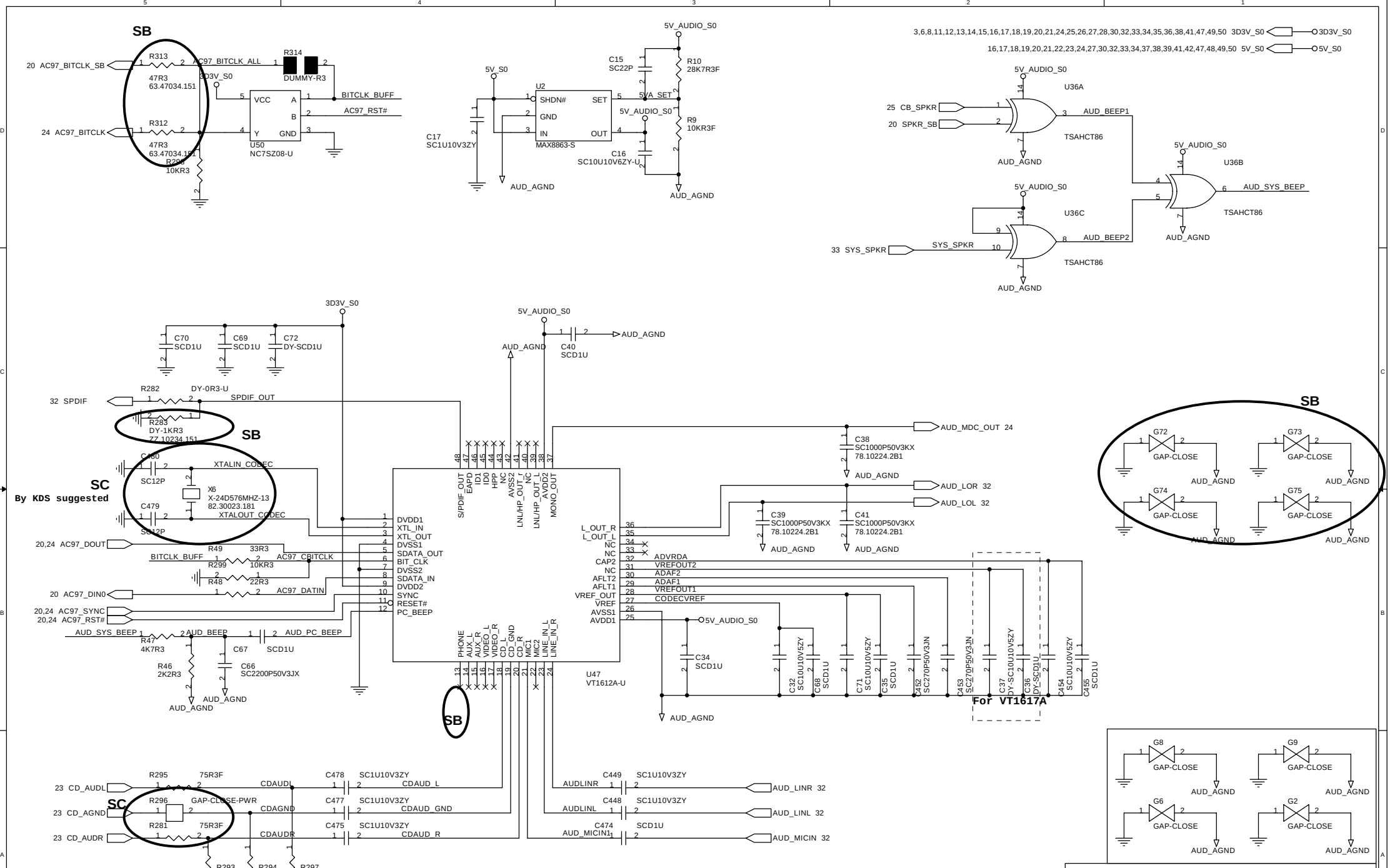
Date: Friday, July 23, 2004 | Sheet 29 of 50

MINI-PCI



By ME requset CN11 P/N:
Main 20.F0222.124
Second 62.10034.031

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MINI-PCI***	
Size A3	Document Number EGRET	Rev SC
Date: Friday, July 23, 2004	Sheet 30 of 50	



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AUDIO (1/2) -- CODEC VT1612A***

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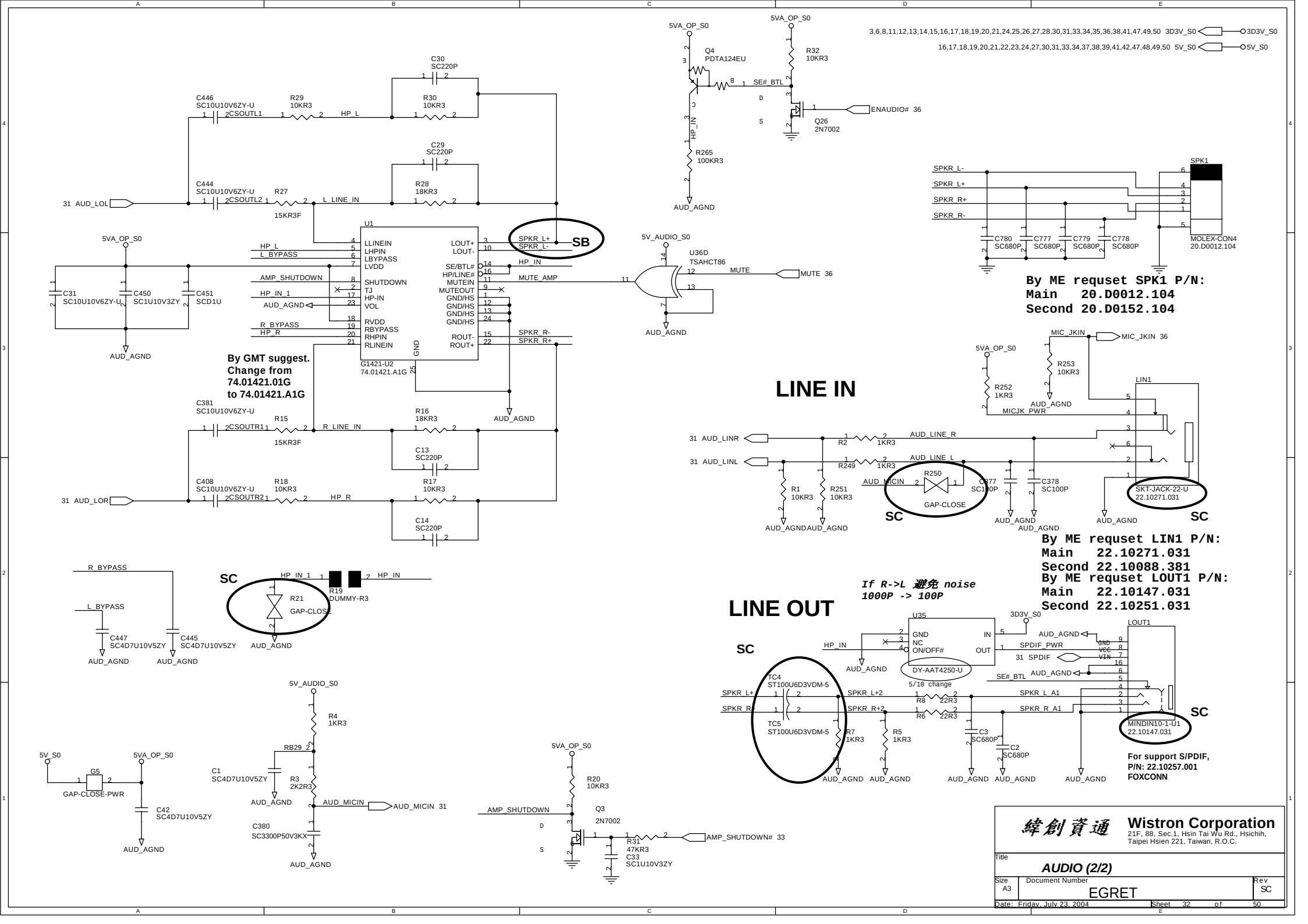
Date: Friday, July 23, 2004 Sheet 31 of 50


3,6,8,11,12,13,14,15,16,17,18,19,20,21,24,25,26,27,28,30,31,33,34,35,36,38,41,47,49,50 3D3V_S0
16,17,18,19,20,21,22,23,24,27,30,31,33,34,37,38,39,41,42,47,48,49,50 5V_S0
5VA_OP_S0
Q4
PDTA124EU
R32
10KR3
SE# BTL
ENAUDIO# 36
Q26
2N7002
HP_IN
R265
100KR3
AUD_AGND
C30
SC220P
C446
SC10U10V6ZY-U
R29
10KR3
HP_L
R30
10KR3
C29
SC220P
C444
SC10U10V6ZY-U
R27
15KR3F
L_LINE_IN
R28
18KR3
31 AUD_LOL
U1
LLINEIN
LHPIN
LBYPASS
LVDD
SHUTDOWN
TJ
HP-IN
VOL
RVDD
RBYPASS
RHPIN
RLINEIN
LOUT+
LOUT-
SE/BTL#
HP/LINE#
MUTEIN
MUTEOUT
GND/HS
ROUT-
ROUT+
GND
SPKR_L+
SPKR_L-
SB
HP_IN
MUTE_AMP
AMP_SHUTDOWN
HP_IN_1
R_BYPASS
HP_R
G1421-U2
74.01421.A1G
5V_AUDIO_S0
U36D
TSAHCT86
MUTE
MUTE 36
C31
SC10U10V6ZY-U
C450
SC1U10V3ZY
C451
SCD1U
By GMT suggest.
Change from
74.01421.01G
to 74.01421.A1G
C381
SC10U10V6ZY-U
R15
15KR3F
R_LINE_IN
R16
18KR3
C13
SC220P
C408
SC10U10V6ZY-U
R18
10KR3
R17
10KR3
31 AUD_LOR
C14
SC220P
SPKR_R-
SPKR_R+
SPK1
SPKR_L-
SPKR_L+
SPKR_R+
SPKR_R-
C780
SC680P
C777
SC680P
C779
SC680P
C778
SC680P
MOLEX-CON4
20.D0012.104
By ME requset SPK1 P/N:
Main 20.D0012.104
Second 20.D0152.104
LINE IN
MIC_JKIN
MIC_JKIN 36
R252
1KR3
R253
10KR3
MICJK_PWR
LIN1
31 AUD_LINR
31 AUD_LINL
R2
1KR3
R249
1KR3
AUD_LINE_R
AUD_LINE_L
R250
AUD_MICIN
GAP-CLOSE
SC
R1
10KR3
R251
10KR3
C377
SC100P
C378
SC100P
SKT-JACK-22-U
22.10271.031
By ME requset LIN1 P/N:
Main 22.10271.031
Second 22.10088.381
By ME requset LOUT1 P/N:
Main 22.10147.031
Second 22.10251.031
R_BYPASS
L_BYPASS
C447
SC4D7U10V5ZY
C445
SC4D7U10V5ZY
HP_IN_1
HP_IN
R19
DUMMY-R3
R21
GAP-CLOSE
LINE OUT
If R->L 避免 noise
1000P -> 100P
U35
GND
NC
ON/OFF#
IN
OUT
DY-AAT4250-U
5/10 change
3D3V_S0
LOUT1
SPDIF_PWR
31 SPDIF
SE# BTL
TC4
ST100U6D3VDM-5
TC5
ST100U6D3VDM-5
SPKR_L+2
SPKR_R+2
R8
22R3
R6
22R3
R7
1KR3
R5
1KR3
C3
SC680P
C2
SC680P
SPKR_L_A1
SPKR_R_A1
MINDIN10-1-U1
22.10147.031
For support S/PDIF,
P/N: 22.10257.001
FOXCONN
5V_S0
G5
GAP-CLOSE-PWR
C42
SC4D7U10V5ZY
R4
1KR3
RB29
C1
SC4D7U10V5ZY
R3
2K2R3
AUD_MICIN
AUD_MICIN 31
C380
SC3300P50V3KX
R20
10KR3
Q3
2N7002
R31
47KR3
C33
SC1U10V3ZY
AMP_SHUTDOWN# 33
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO (2/2)
Size
A3
Document Number
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Rev
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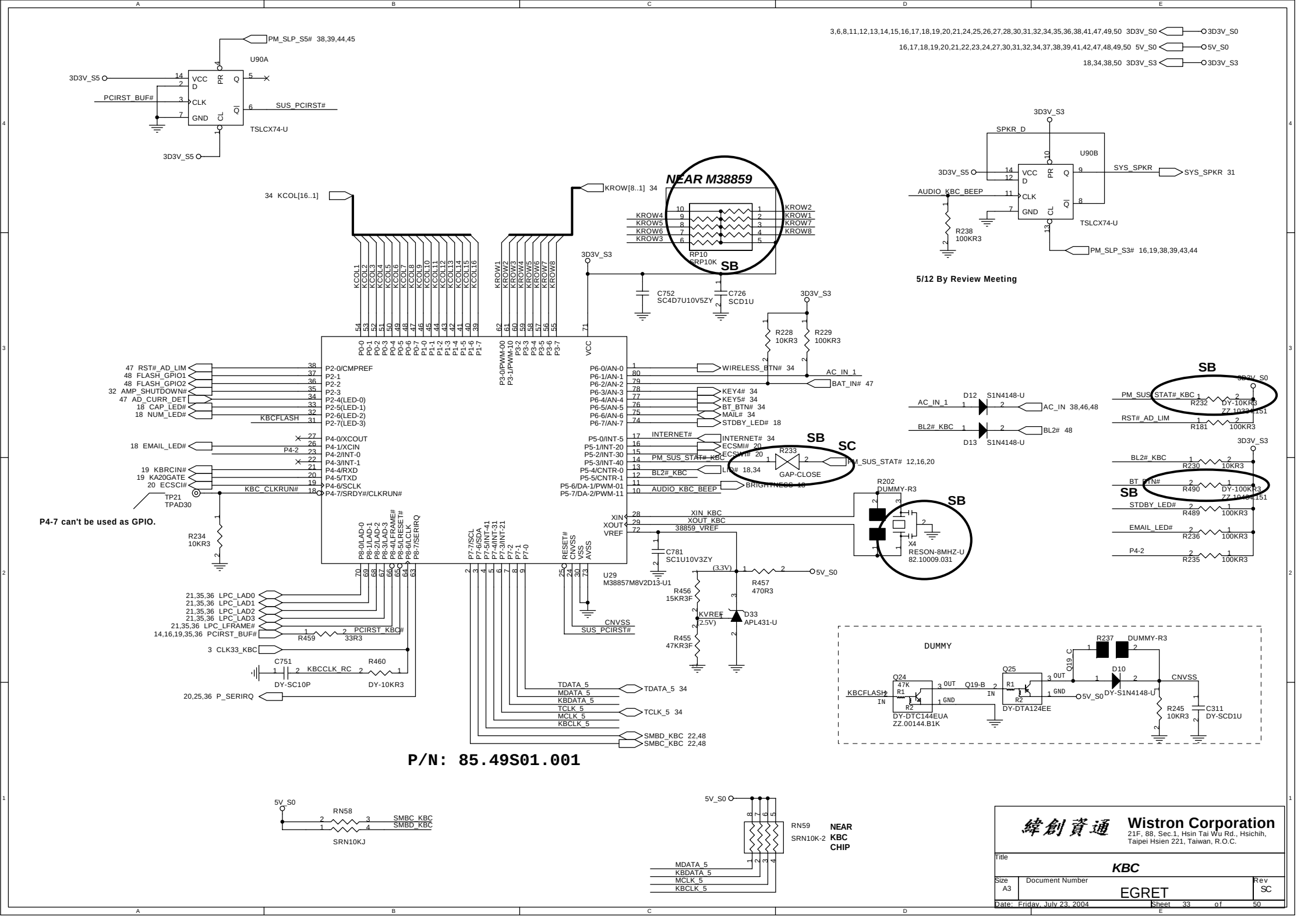
U90A
TSLCX74-U
PM_SLP_S5# 38,39,44,45
3D3V_S5
PCIRST_BUF#
SUS_PCIRST#
3,6,8,11,12,13,14,15,16,17,18,19,20,21,24,25,26,27,28,30,31,32,34,35,36,38,41,47,49,50 3D3V_S0
16,17,18,19,20,21,22,23,24,27,30,31,32,34,37,38,39,41,42,47,48,49,50 5V_S0
18,34,38,50 3D3V_S3
3D3V_S0
5V_S0
3D3V_S3
SPKR_D
U90B
SYS_SPKR
SYS_SPKR 31
AUDIO_KBC_BEEP
R238
100KR3
PM_SLP_S3# 16,19,38,39,43,44
5/12 By Review Meeting
NEAR M38859
34 KCOL[16..1]
KROW[8..1] 34
RP10
SRP10K
SB
C752
SC4D7U10V5ZY
C726
SCD1U
R228
10KR3
R229
100KR3
47 RST#_AD_LIM
48 FLASH_GPIO1
48 FLASH_GPIO2
32 AMP_SHUTDOWN#
47 AD_CURR_DET
18 CAP_LED#
18 NUM_LED#
KBCFLASH
P2-0/CMPREF
P2-1
P2-2
P2-3
P2-4(LED-0)
P2-5(LED-1)
P2-6(LED-2)
P2-7(LED-3)
WIRELESS_BTN# 34
AC_IN_1
BAT_IN# 47
KEY4# 34
KEY5# 34
BT_BTN# 34
MAIL# 34
STDBY_LED# 18
18 EMAIL_LED#
P4-2
P4-0/XCOUT
P4-1/XCIN
P4-2/INT-0
P4-3/INT-1
P4-4/RXD
P4-5/TXD
P4-6/SCLK
P4-7/SRDY#/CLKRUN#
19 KBRCIN#
19 KA20GATE
20 ECSCI#
KBC_CLKRUN#
TP21
TPAD30
P4-7 can't be used as GPIO.
R234
10KR3
P5-0/INT-5
P5-1/INT-20
P5-2/INT-30
P5-3/INT-40
P5-4/CNTR-0
P5-5/CNTR-1
P5-6/DA-1/PWM-01
P5-7/DA-2/PWM-11
INTERNET#
INTERNET# 34
ECSMI# 20
ECSWI# 20
PM_SUS_STAT#_KBC
PM_SUS_STAT# 12,16,20
BL2# KBC
LID# 18,34
AUDIO_KBC_BEEP
BRIGHTNESS 18
R233
GAP-CLOSE
SC
D12
S1N4148-U
D13
S1N4148-U
AC_IN_1
AC_IN 38,46,48
BL2# KBC
BL2# 48
R232
DY-10KR3
ZZ.10224.151
RST#_AD_LIM
R181
100KR3
R230
10KR3
BT_BTN#
R490
DY-100KR3
ZZ.10184.151
STDBY_LED#
R489
100KR3
EMAIL_LED#
R236
100KR3
P4-2
R235
100KR3
R202
DUMMY-R3
X4
RESON-8MHZ-U
82.10009.031
XIN
XOUT
VREF
XIN_KBC
XOUT_KBC
38859_VREF
C781
SC1U10V3ZY
U29
M38857M8V2D13-U1
R456
15KR3F
R457
470R3
5V_S0
KVREF
(2.5V)
D33
APL431-U
R455
47KR3F
CNVSS
SUS_PCIRST#
21,35,36 LPC_LAD0
21,35,36 LPC_LAD1
21,35,36 LPC_LAD2
21,35,36 LPC_LAD3
21,35,36 LPC_LFRAME#
14,16,19,35,36 PCIRST_BUF#
R459
33R3
PCIRST_KBC#
3 CLK33_KBC
C751
DY-SC10P
KBCCLK_RC
R460
DY-10KR3
20,25,36 P_SERIRQ
TDATA_5
MDATA_5
KBDATA_5
TCLK_5
MCLK_5
KBCLK_5
TDATA_5 34
TCLK_5 34
SMBD_KBC 22,48
SMBC_KBC 22,48
DUMMY
Q24
47K
R1
R2
DY-DTC144EUA
ZZ.00144.B1K
KBCFLASH
Q19-B
Q25
DY-DTA124EE
R237
DUMMY-R3
Q19-C
D10
DY-S1N4148-U
CNVSS
R245
10KR3
C311
DY-SCD1U
5V_S0
RN58
SMBC_KBC
SMBD_KBC
SRN10KJ
RN59
SRN10K-2
NEAR
KBC
CHIP
MDATA_5
KBDATA_5
MCLK_5
KBCLK_5
P/N: 85.49S01.001
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC
Size
A3
Document Number
EGRET
Rev
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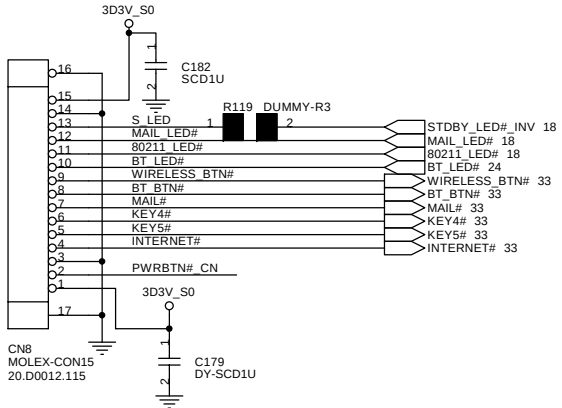
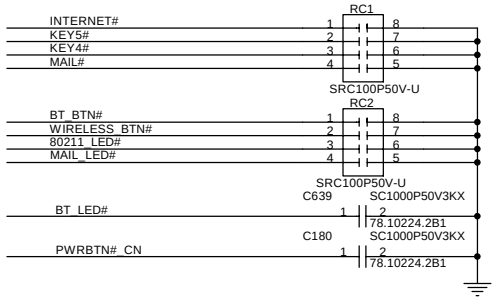
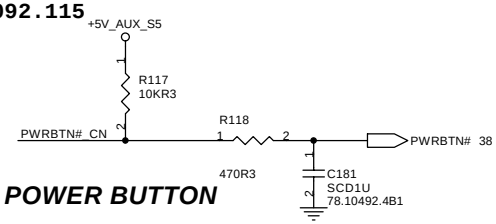
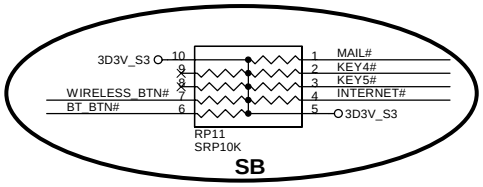




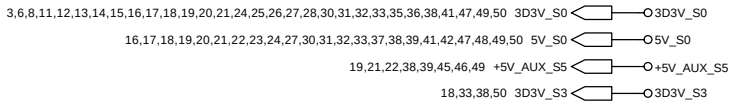
By ME requset CN8 P/N:
Main 20.D0012.115
Second 20.D0092.115

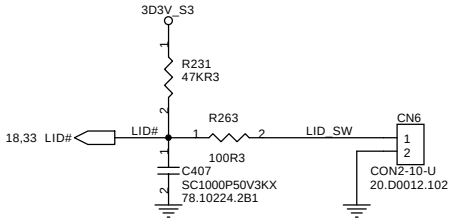


POWER BUTTON

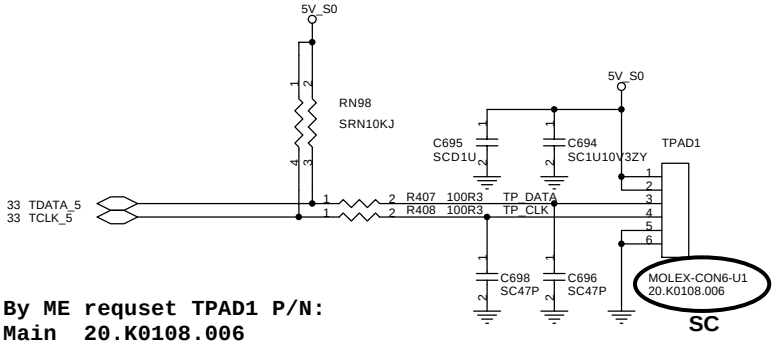


Launch Board CONN





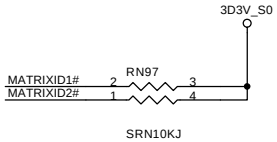
Cover Up Switch



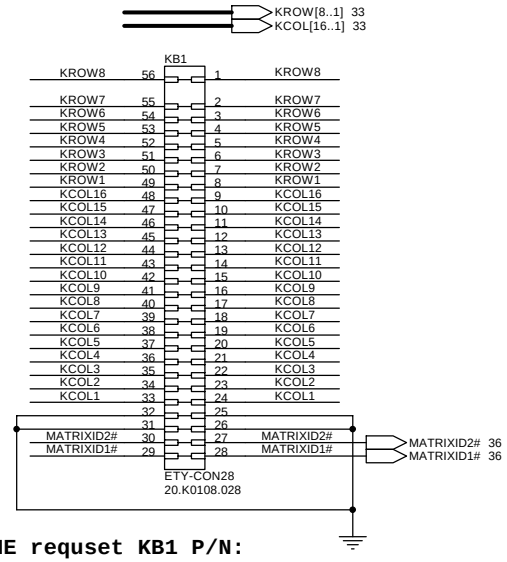
By ME requset TPAD1 P/N:
Main 20.K0108.006
Second 20.K0021.006

TOUCH PAD

Internal KeyBoard CONN

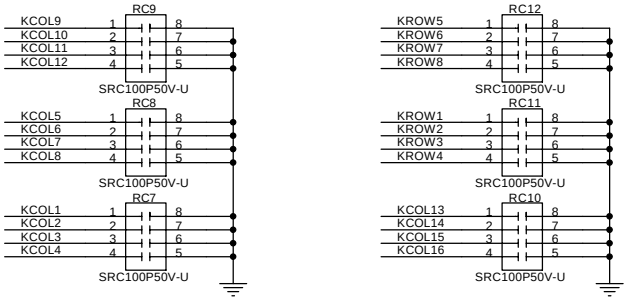


Keyboard matrix	(from	vendor)		
	US	Jap	Eur	Other
Low Bit MATRIXID1#	1	1	0	0
High Bit MATRIXID2#	1	0	1	0



By ME requset KB1 P/N:
Main 20.K0108.028
Second 20.K0021.028

EMI Bypass cap.



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LAUNCH / TOUCHPAD / KB CONN***

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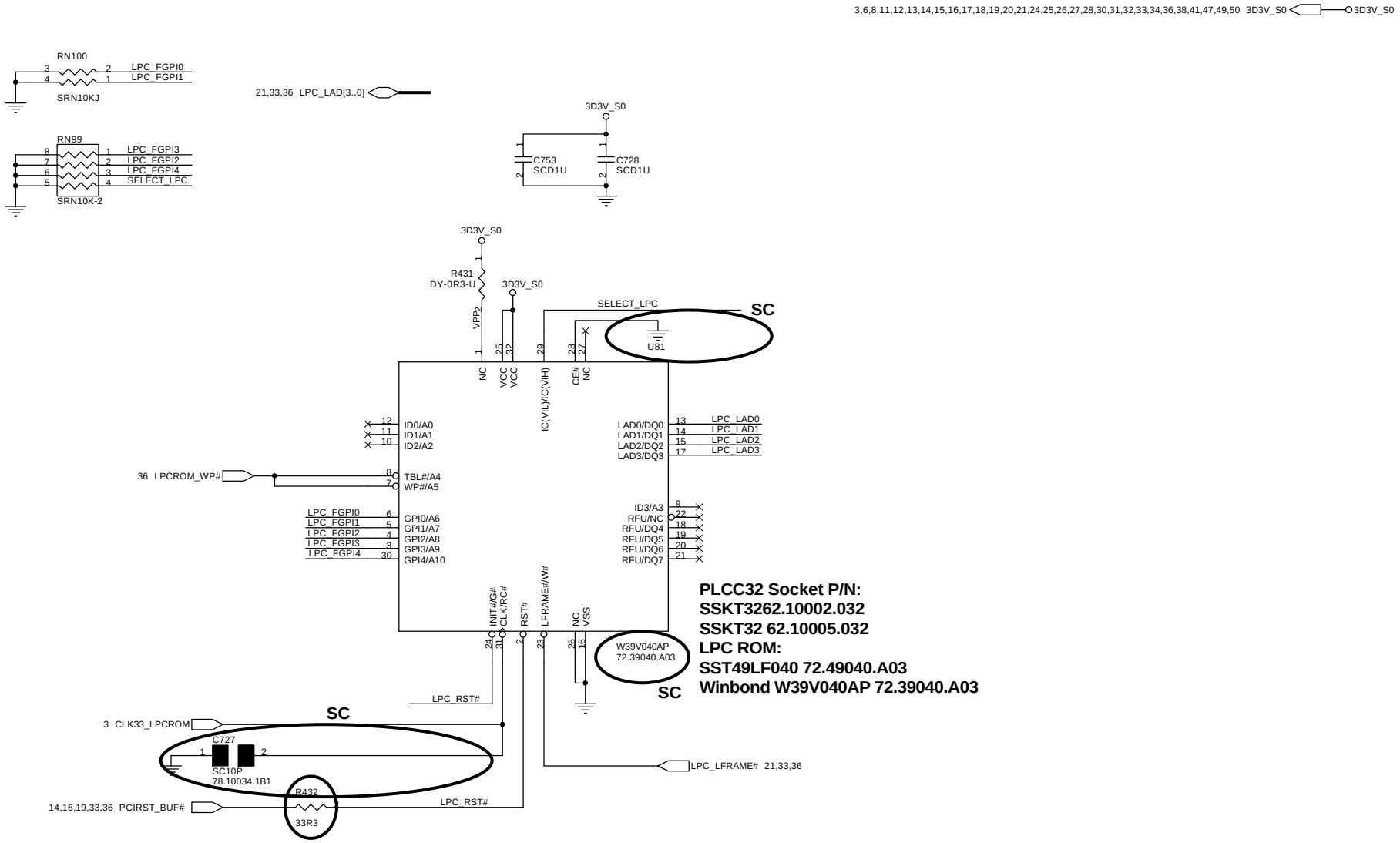

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***LPCROM / DEBUG PORT***	
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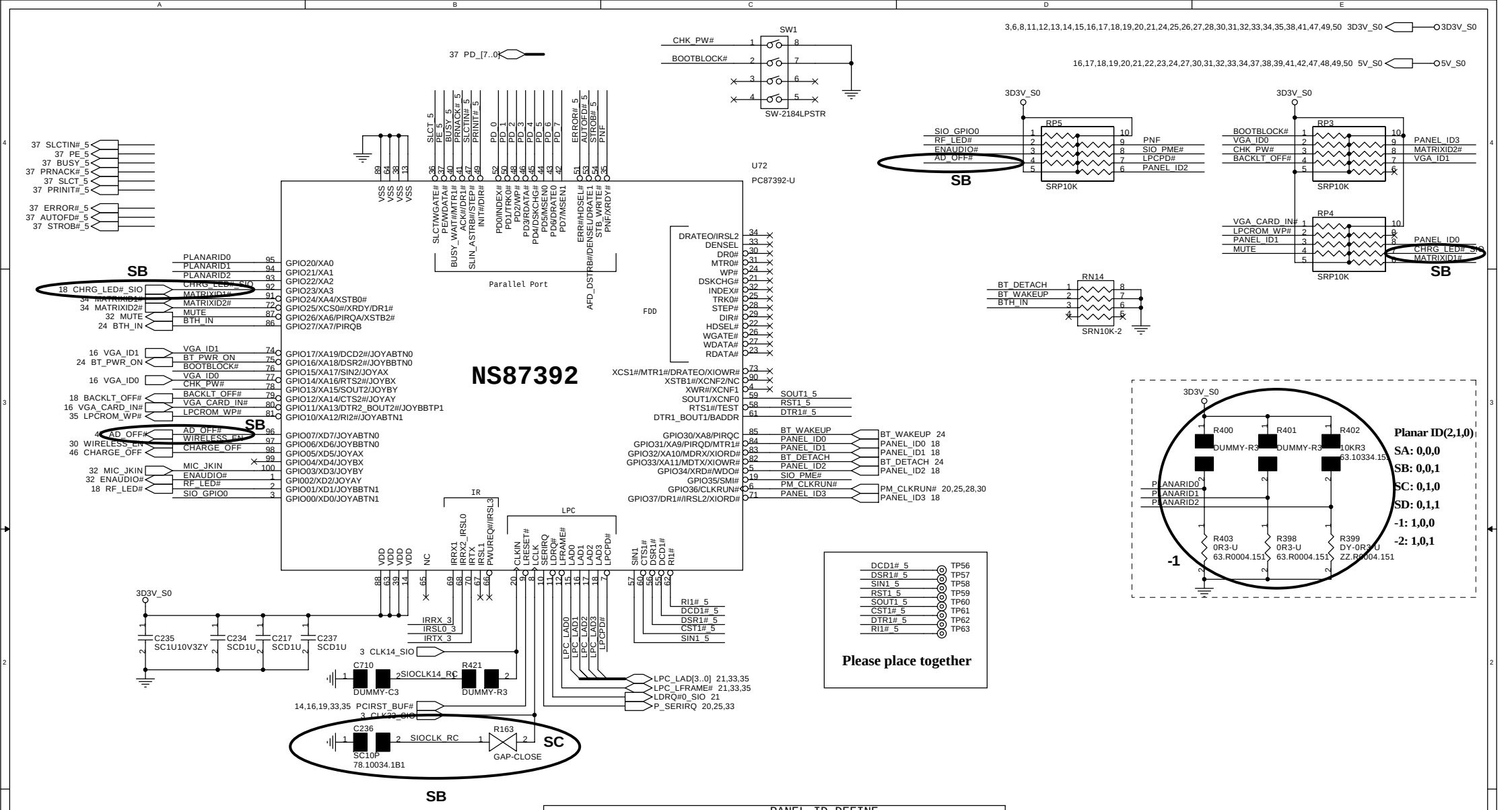
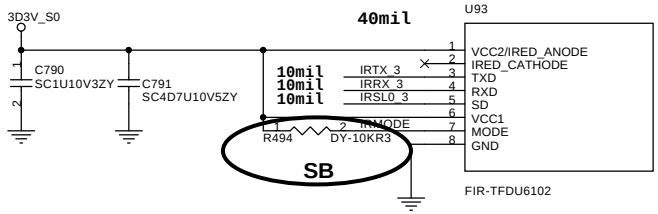


Infineon FIR Module



PANEL ID DEFINE				
PANEL_ID3	PANEL_ID2	PANEL_ID1	PANEL_ID0	VENDORS
0	0	0	0	15" SXGA+
0	0	0	1	Hydis (14")SPWG
0	0	1	0	15" WIDE
0	0	1	1	Hitachi (15")
0	0	1	1	AU (15")
0	0	1	1	CMO(15")
0	1	0	0	CMO(14")
0	1	0	1	AU (14")
0	1	1	0	AU (14")**
0	1	1	1	No Panel

Note : AU (友達),CMO(奇美),** : With Digitizer

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **SUPER IO**

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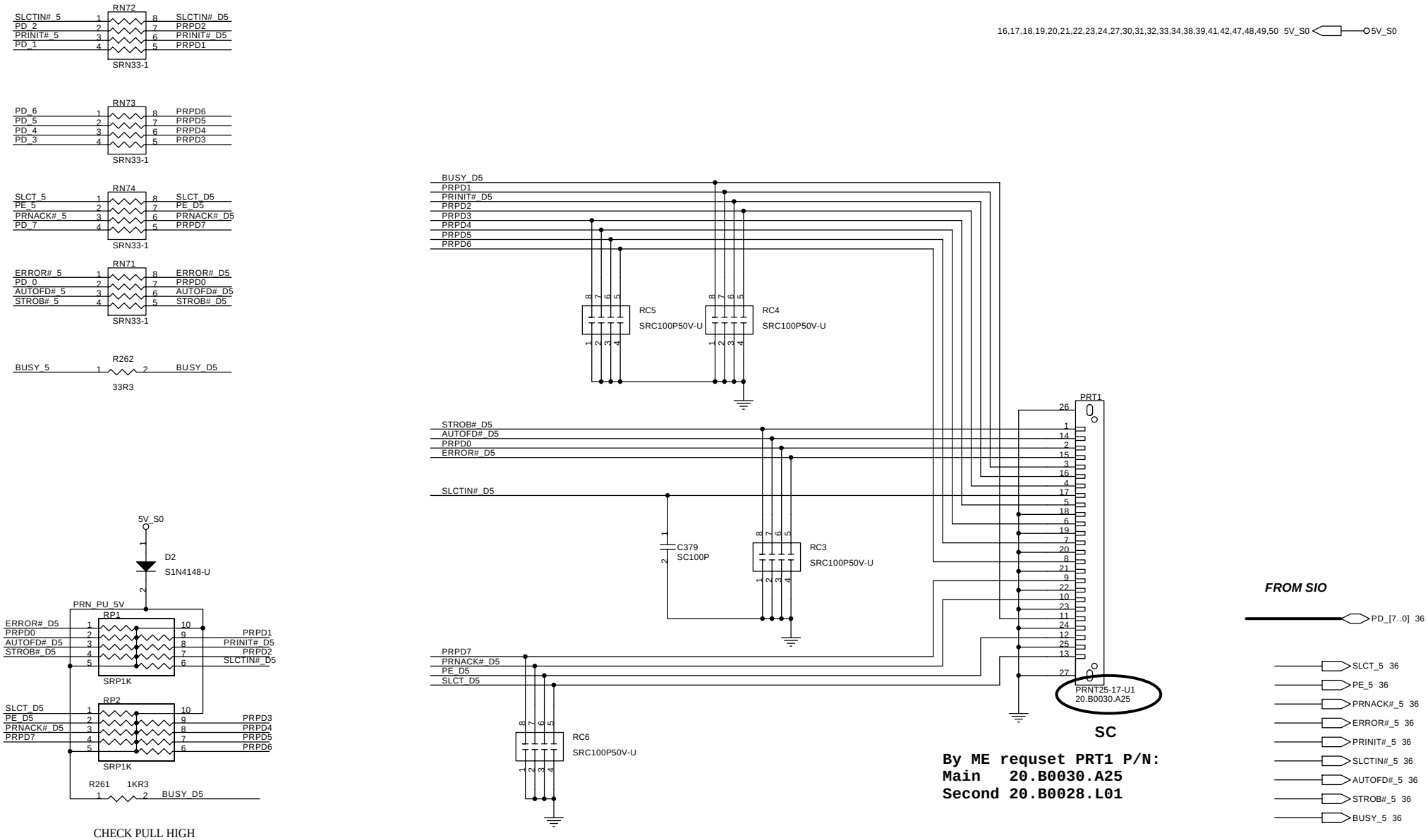
PRINTER PORT



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Title	***Printer PORT***	
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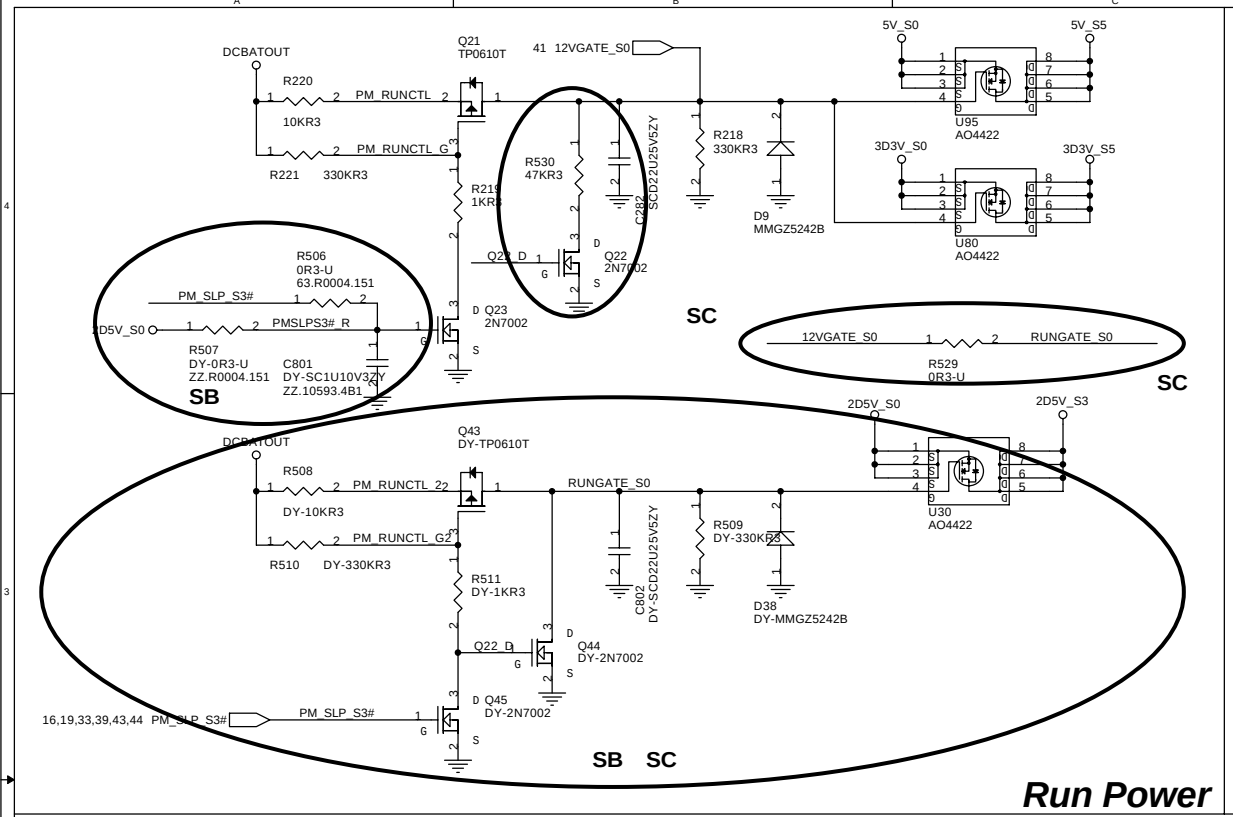
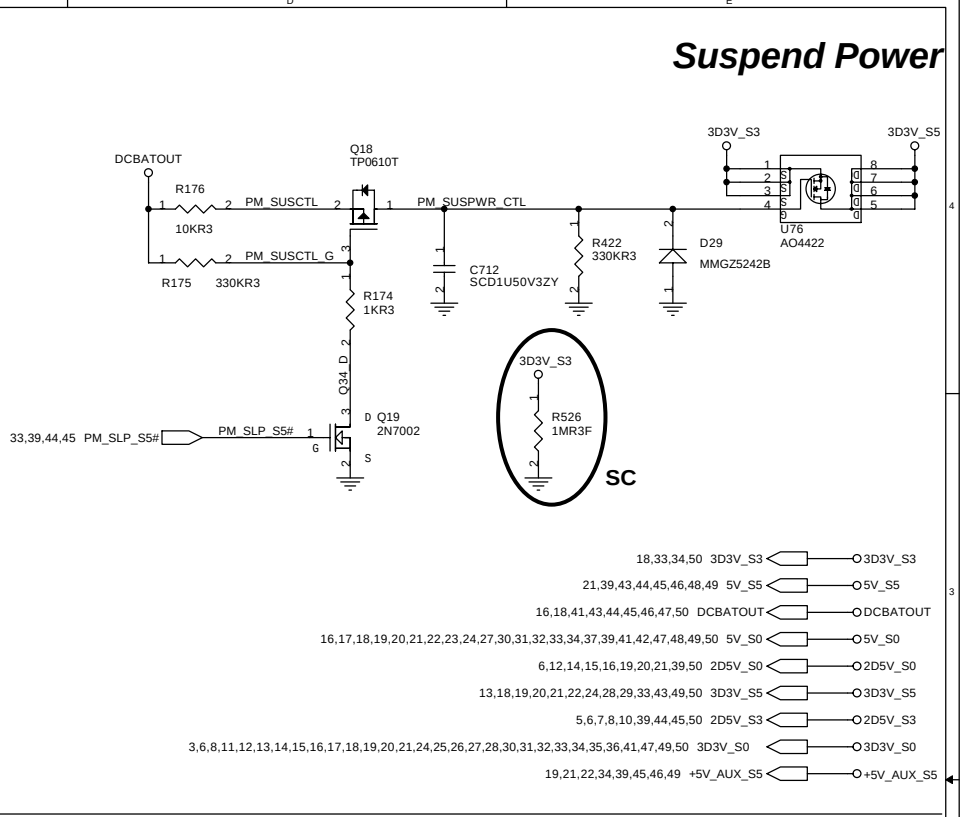
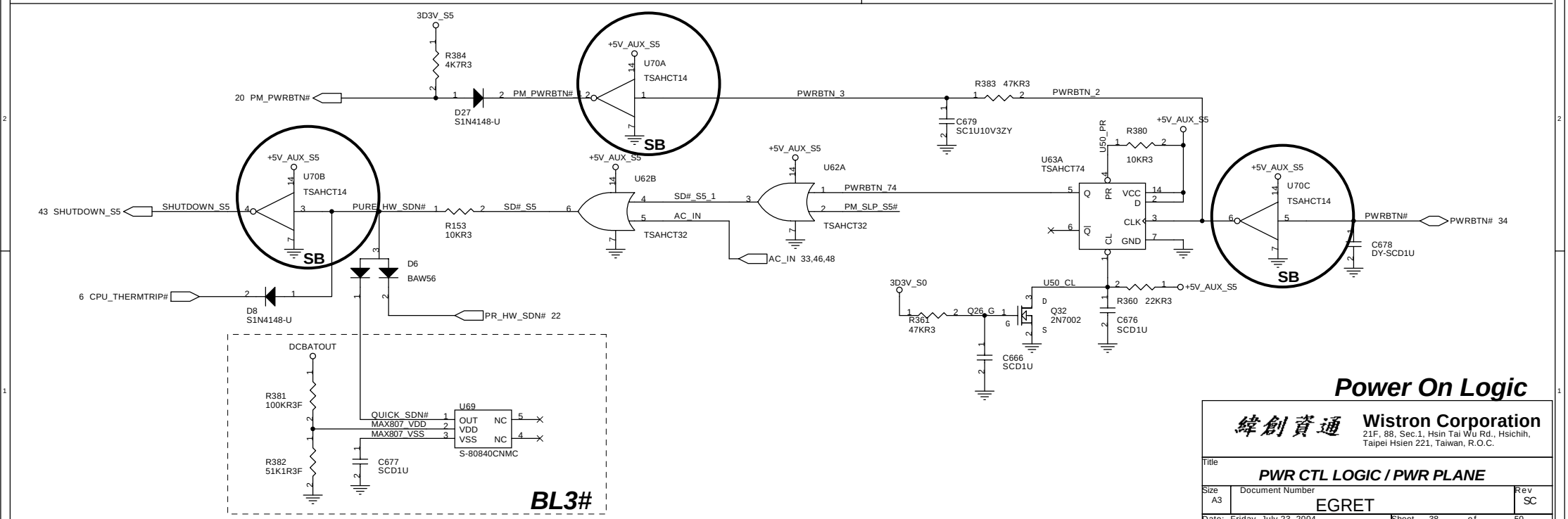


Run Power





Power On Logic

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Title	***PWR CTL LOGIC / PWR PLANE***
Size A3	Document Number EGRET	Rev SC
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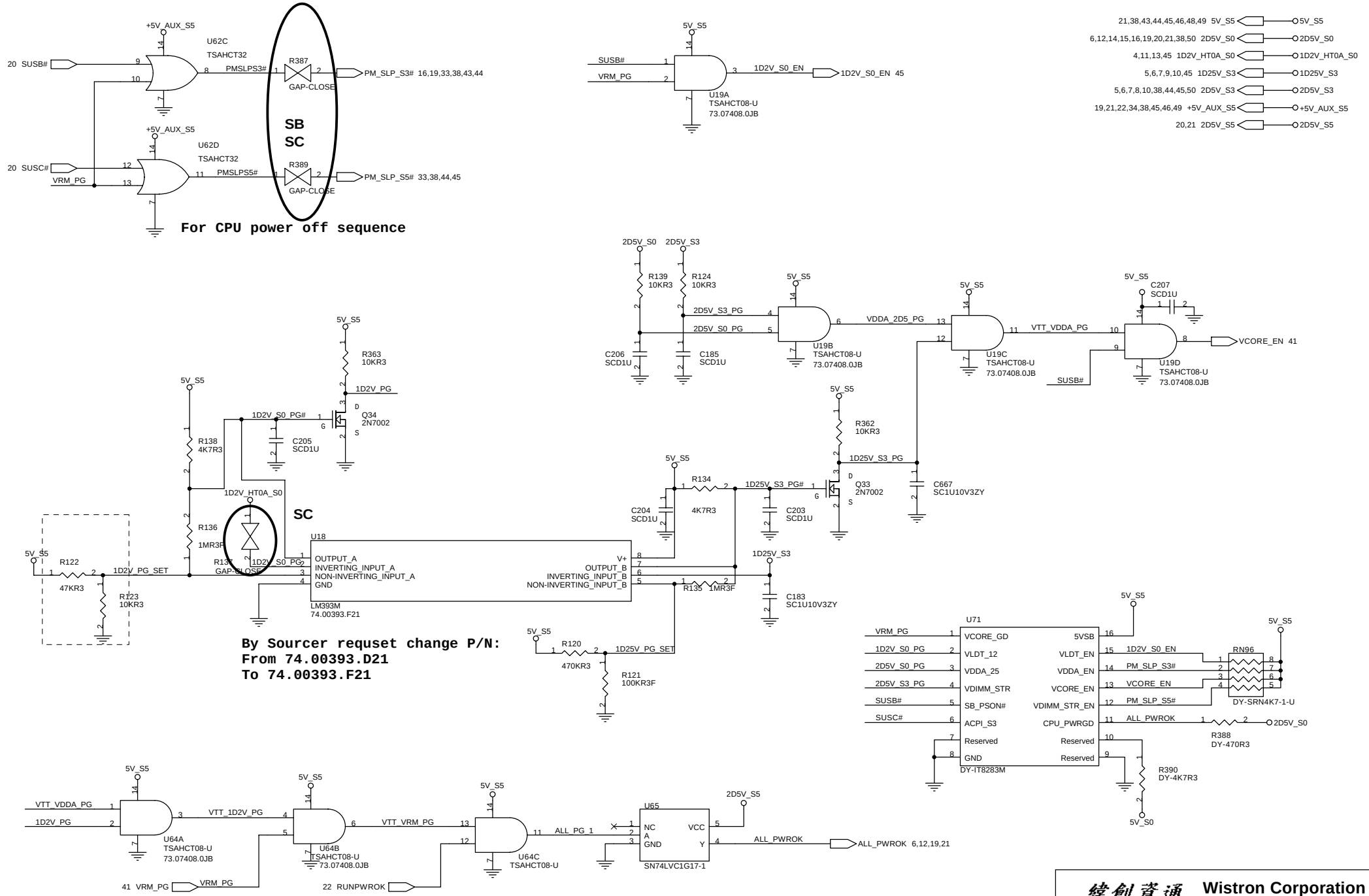

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Title	***POWERGOOD&ENABLES***	
Size: Custom	Document Number: **EGRET**	Rev: SC
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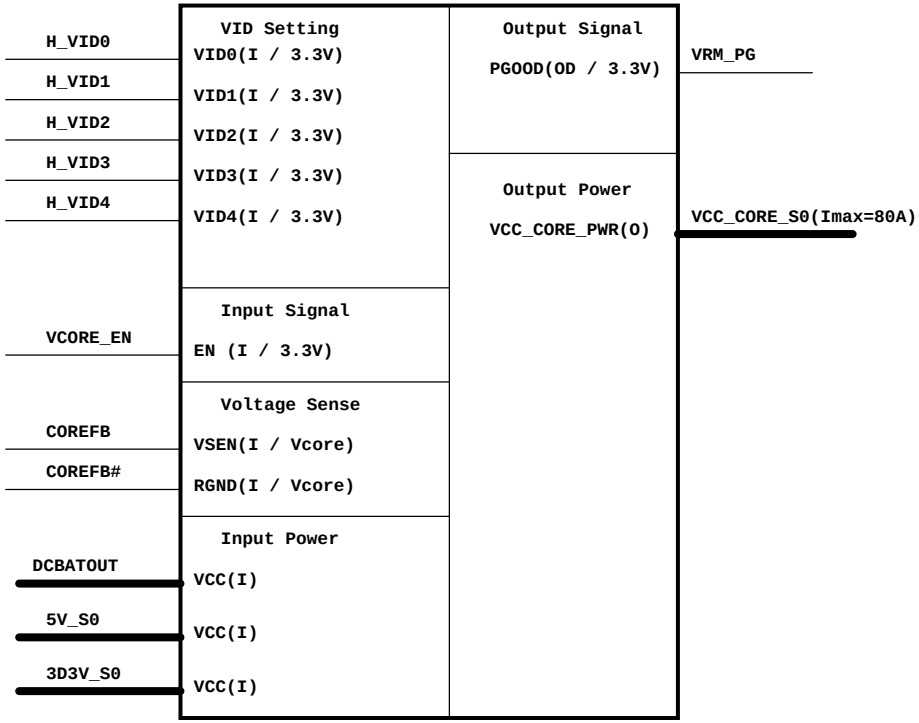
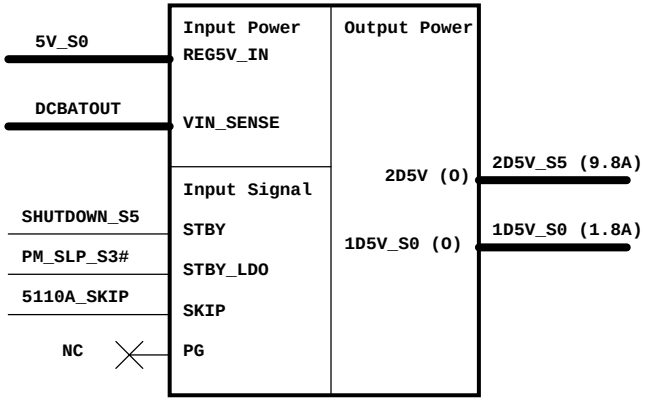
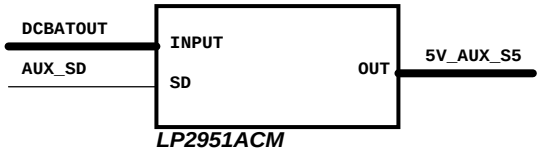
CPU_CORE
Intersil 6559CR + ISL6209CB*2



TI TPS5110
2D5V/1D5V

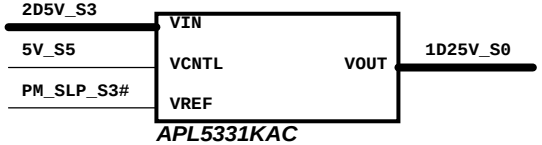


5V_AUX_S5



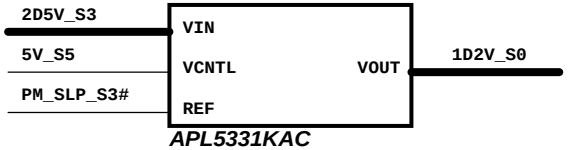
LP2951ACM

1D25V_S3



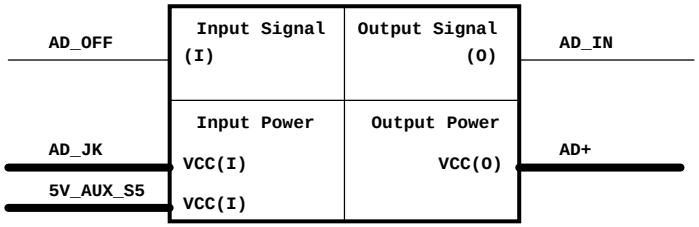
APL5331KAC

1D2V_S0

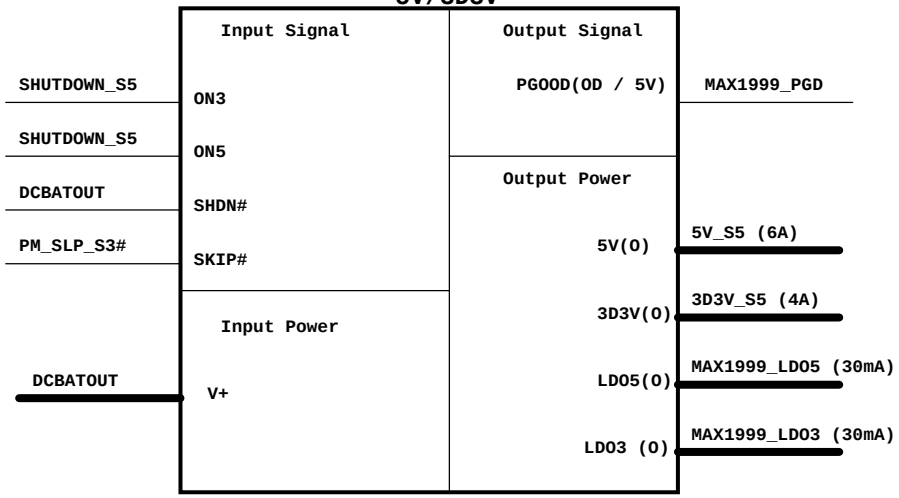


APL5331KAC

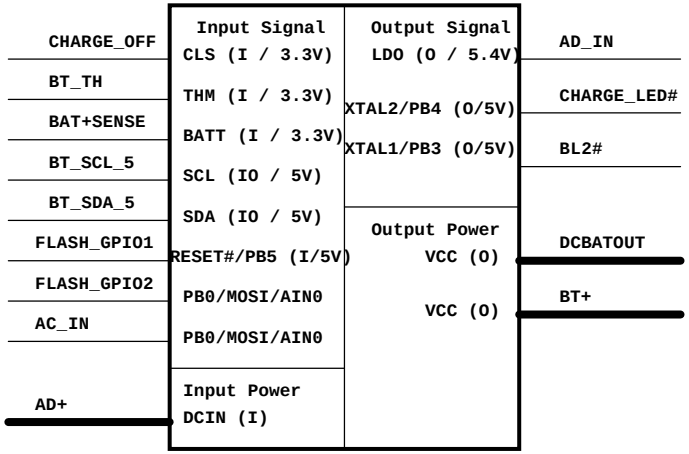
Adapter



Max1999
5V/3D3V



Charger_Max1645 + Tiny12



緯創資通 **Wistron Corporation**
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Title	*Power Block Diagram*	
Size A3	Document Number **EGRET**	Rev SC
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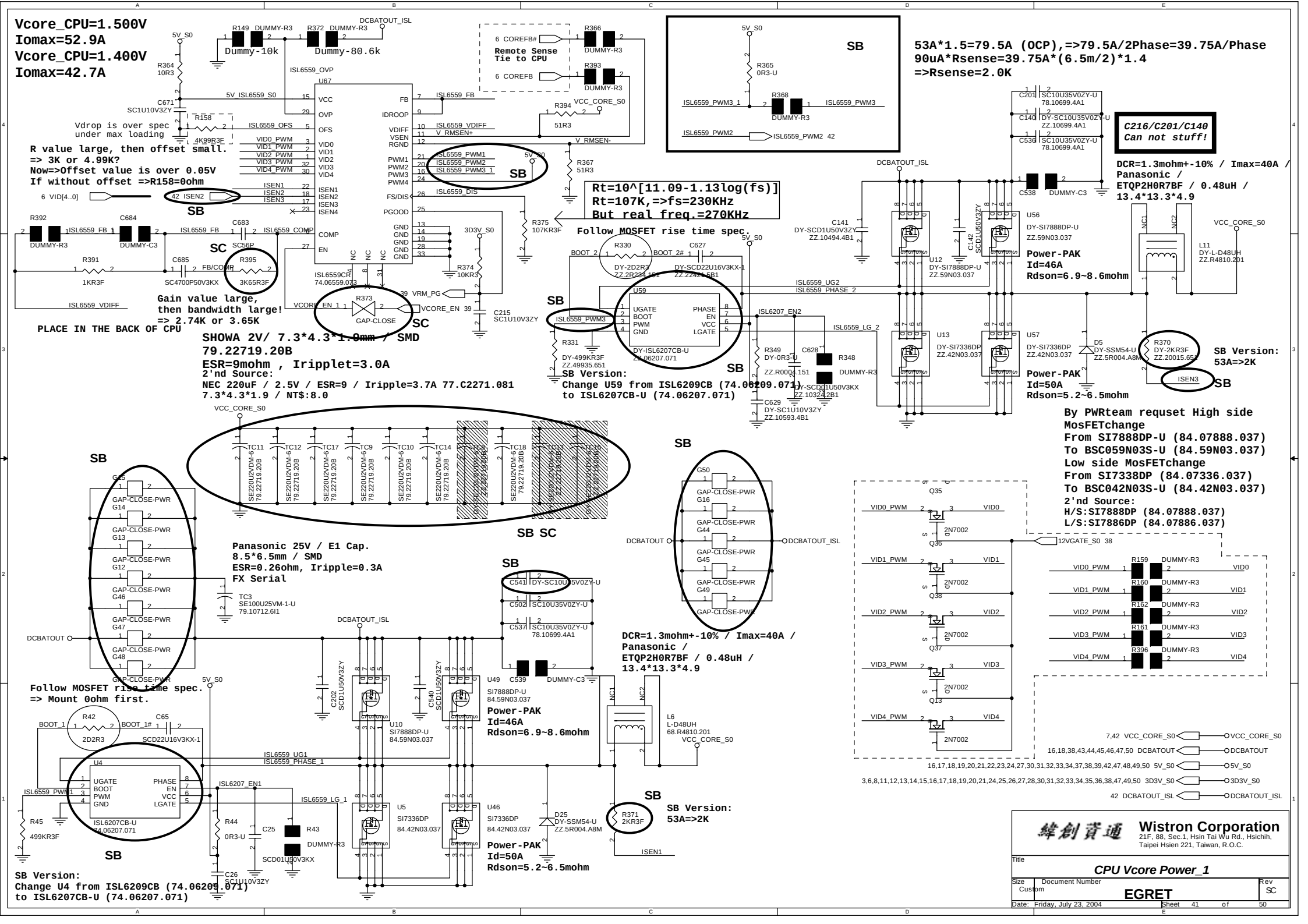
Vcore_CPU=1.500V
Iomax=52.9A
Vcore_CPU=1.400V
Iomax=42.7A
53A*1.5=79.5A (OCP),=>79.5A/2Phase=39.75A/Phase
90uA*Rsense=39.75A*(6.5m/2)*1.4
=>Rsense=2.0K
Remote Sense Tie to CPU
Vdrop is over spec under max loading
R value large, then offset small.
=> 3K or 4.99K?
Now=>Offset value is over 0.05V
If without offset =>R158=0ohm
Rt=10^[11.09-1.13log(fs)]
Rt=107K,=>fs=230KHz
But real freq.=270KHz
Follow MOSFET rise time spec.
C216/C201/C140 Can not stuff!
DCR=1.3mohm+-10% / Imax=40A / Panasonic / ETQP2H0R7BF / 0.48uH / 13.4*13.3*4.9
Power-PAK Id=46A Rdson=6.9~8.6mohm
Power-PAK Id=50A Rdson=5.2~6.5mohm
SB Version: 53A=>2K
Gain value large, then bandwidth large! => 2.74K or 3.65K
PLACE IN THE BACK OF CPU
SHOWA 2V/ 7.3*4.3*1.0mm / SMD
79.22719.20B
ESR=9mohm , Iripplet=3.0A
2'nd Source:
NEC 220uF / 2.5V / ESR=9 / Iripple=3.7A 77.C2271.081
7.3*4.3*1.9 / NT$:8.0
SB Version:
Change U59 from ISL6209CB (74.06209.071)
to ISL6207CB-U (74.06207.071)
By PWRteam requset High side MosFETchange
From SI7888DP-U (84.07888.037)
To BSC059N03S-U (84.59N03.037)
Low side MosFETchange
From SI7338DP (84.07336.037)
To BSC042N03S-U (84.42N03.037)
2'nd Source:
H/S:SI7888DP (84.07888.037)
L/S:SI7886DP (84.07886.037)
Panasonic 25V / E1 Cap.
8.5*6.5mm / SMD
ESR=0.26ohm, Iripple=0.3A
FX Serial
Follow MOSFET rise time spec.
=> Mount 0ohm first.
SB Version:
Change U4 from ISL6209CB (74.06209.071)
to ISL6207CB-U (74.06207.071)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore Power_1
EGRET
Date: Friday, July 23, 2004
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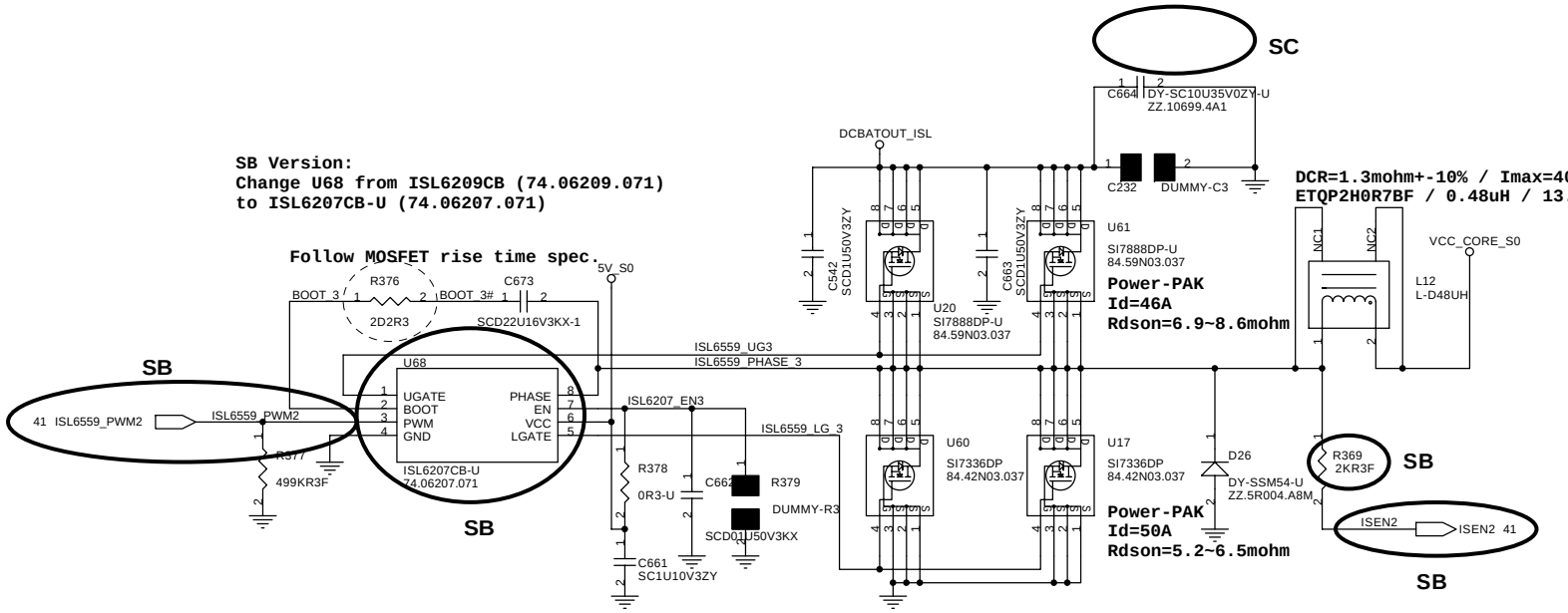

By PWRteam requset High side
MosFETchange
From SI7888DP-U (84.07888.037)
To BSC059N03S-U (84.59N03.037)
Low side MosFETchange
From SI7338DP (84.07336.037)
To BSC042N03S-U (84.42N03.037)

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.300
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	Shutdown

41 DCBATOUT_ISL — DCBATOUT_ISL

7,41 VCC_CORE_S0 — VCC_CORE_S0

16,17,18,19,20,21,22,23,24,27,30,31,32,33,34,37,38,39,41,47,48,49,50 5V_S0 — 5V_S0

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Title: CPU Vcore Power_2

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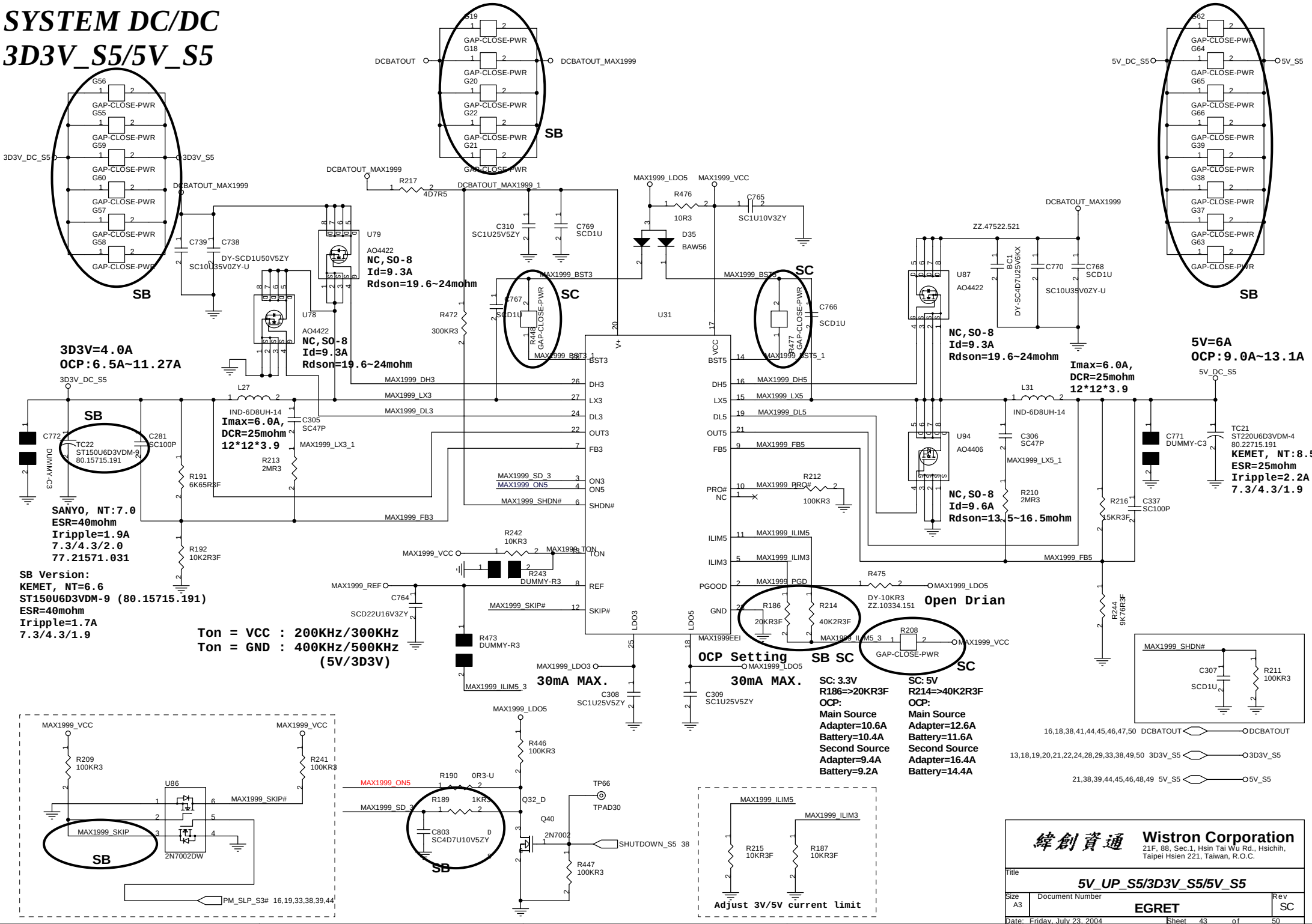
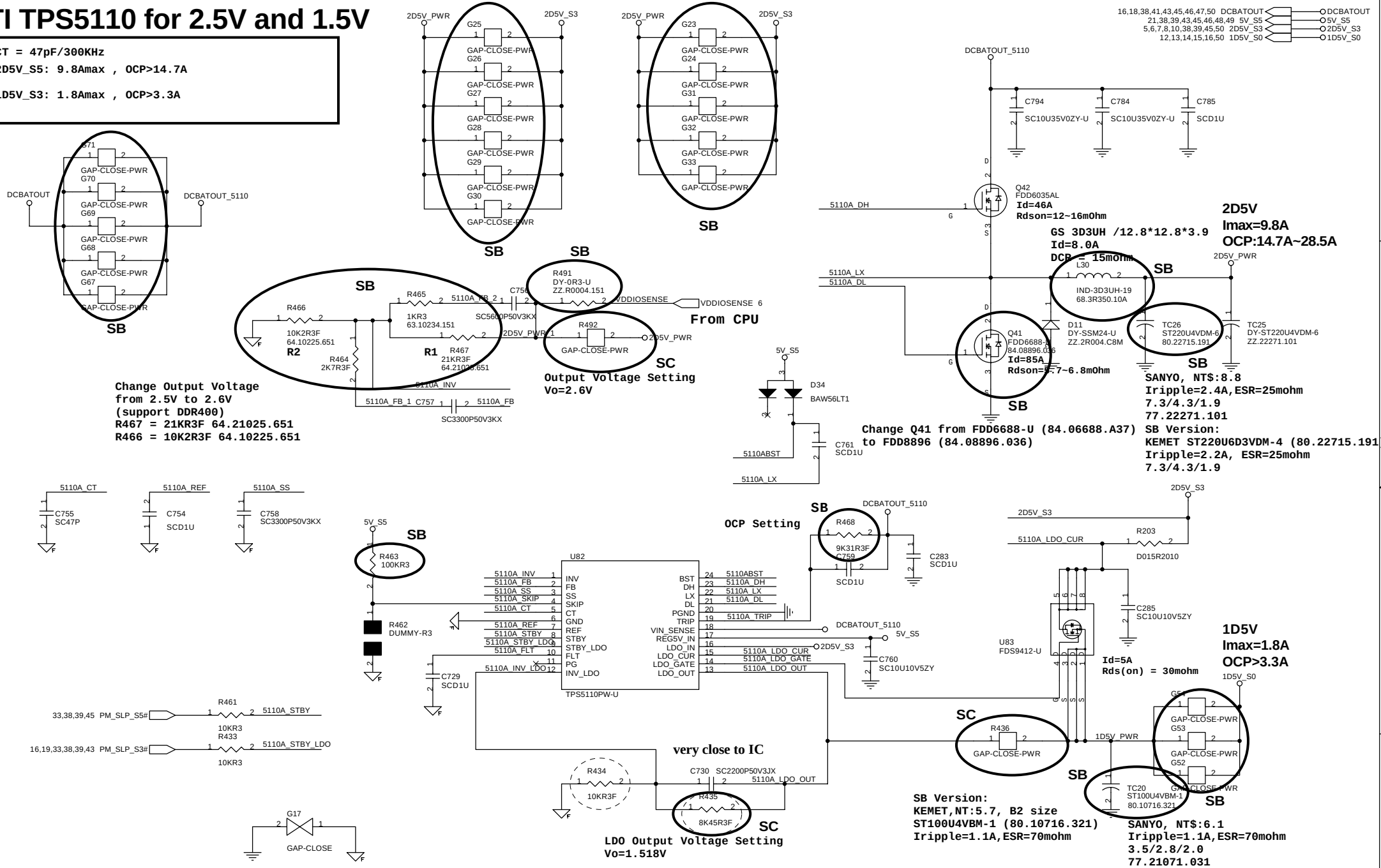
SYSTEM DC/DC
3D3V_S5/5V_S5



TI TPS5110 for 2.5V and 1.5V

CT = 47pF/300KHz
2D5V_S5: 9.8Amax , OCP>14.7A

1D5V_S3: 1.8Amax , OCP>3.3A



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	2D5V_S5/1D5V_S0_TPS5110	
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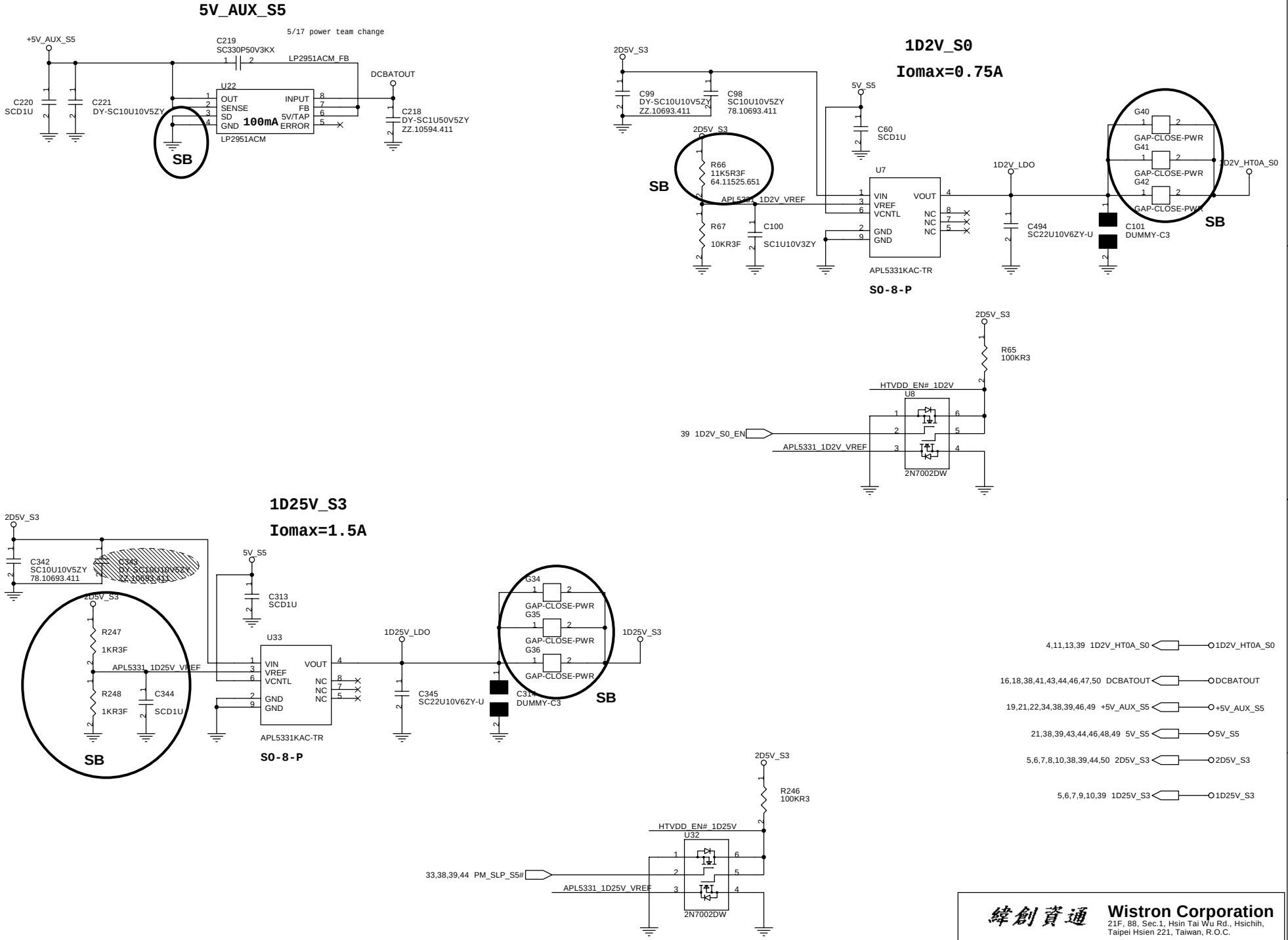

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Title: ***1D25V_LDO/3V_AUX/5V_AUX***

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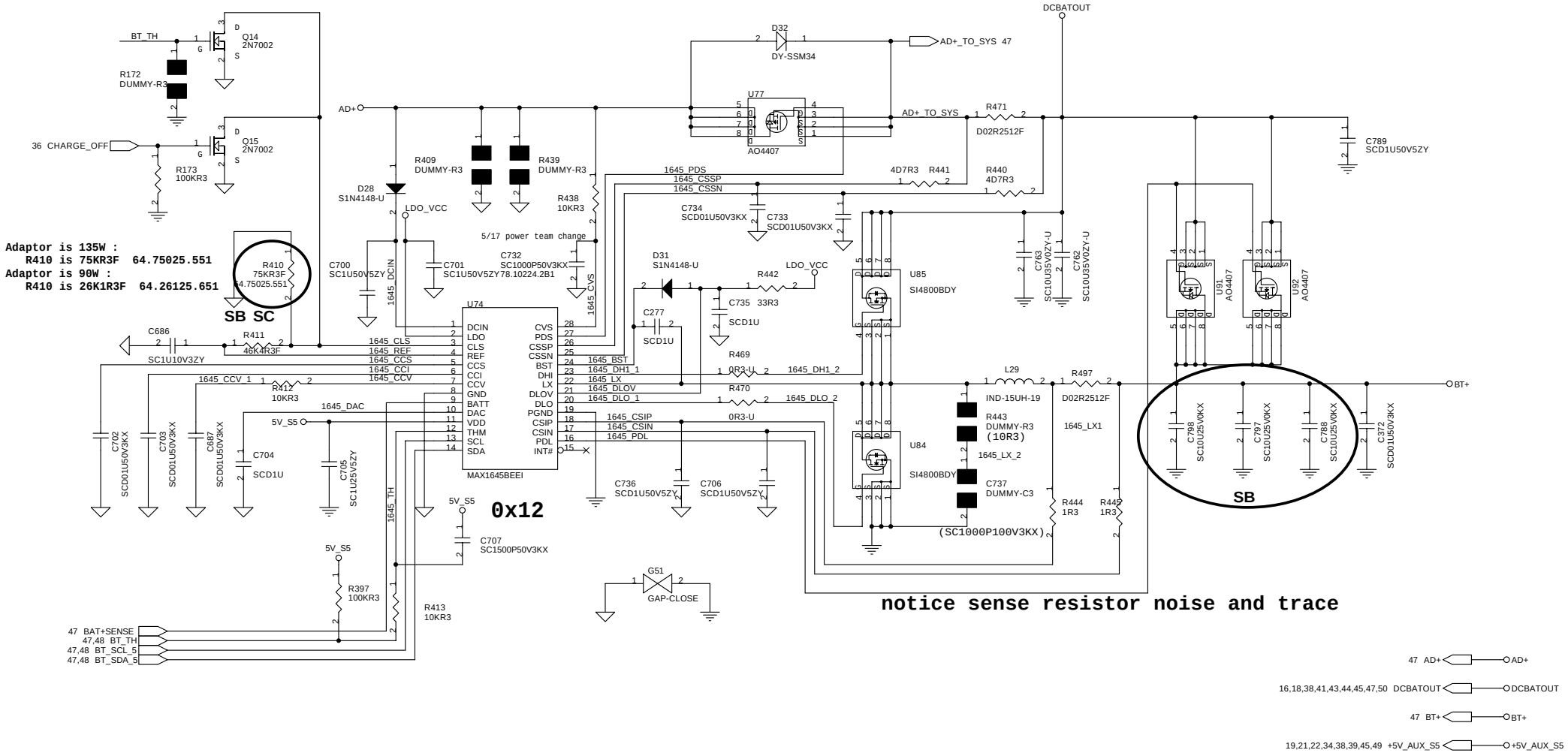

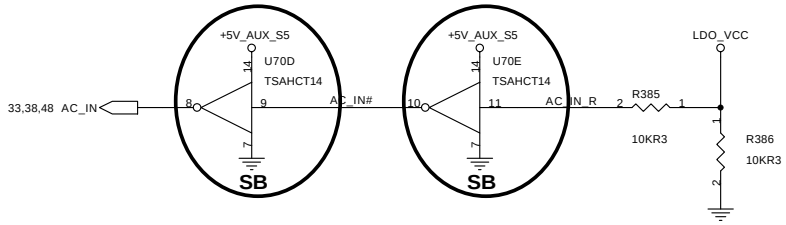

Li-ion =>8 Cells (4S2P*2=16.8V)
Ni-Mh =>8 Cells (8*1.8=14.4V)

Low => Li-ion
(3.3A=2400mAH*2*0.7C)
High => Ni-MH
(2.5A=4800mAH*0.55C)

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Title	***CHARGER MAX1645***	
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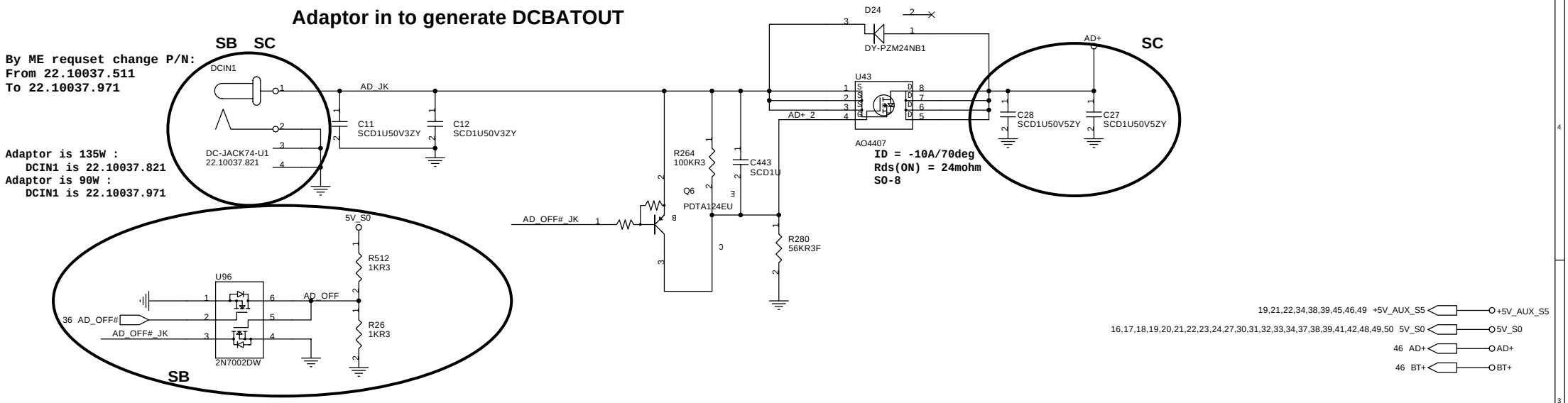
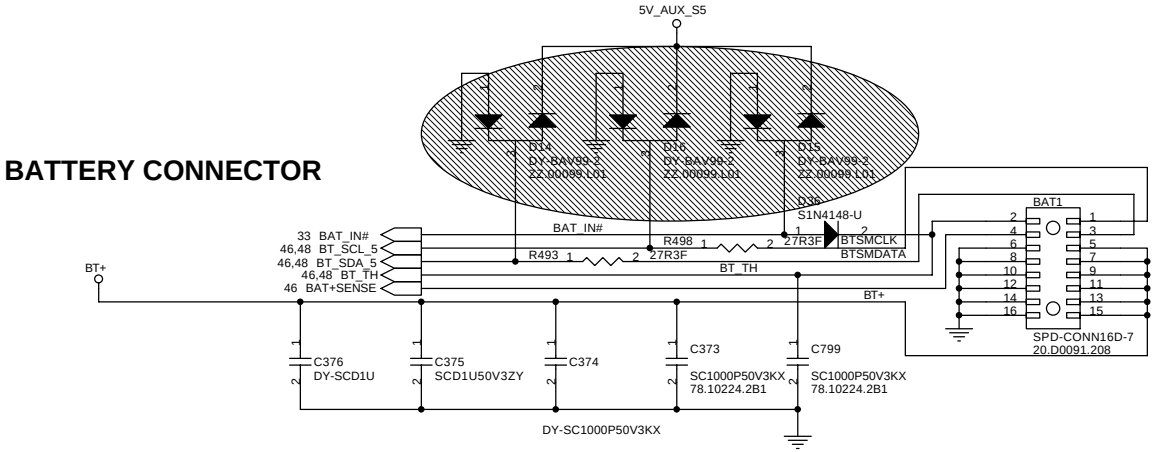
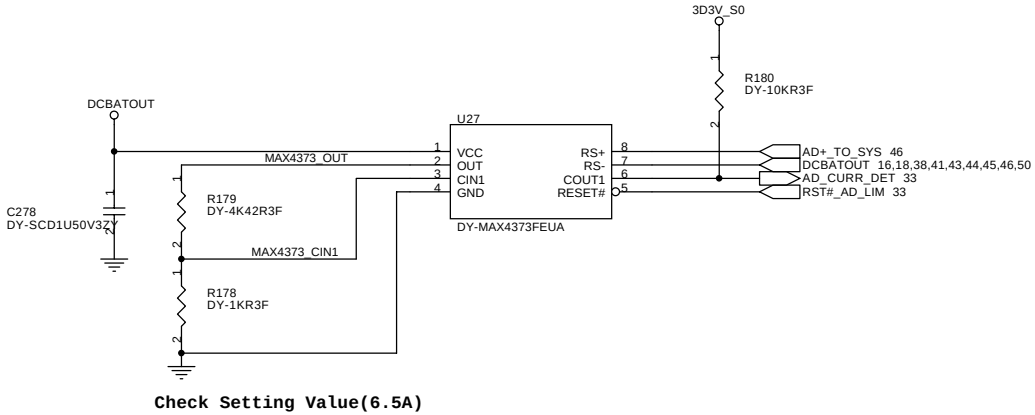
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR





Check Setting Value(6.5A)

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Taipei Hsien 221, Taiwan, R.O.C.

Title	***DC/DC (1/2) -- 5V / 3.3V / 2.5V***	
Size A3	Document Number EGRET	Rev SC
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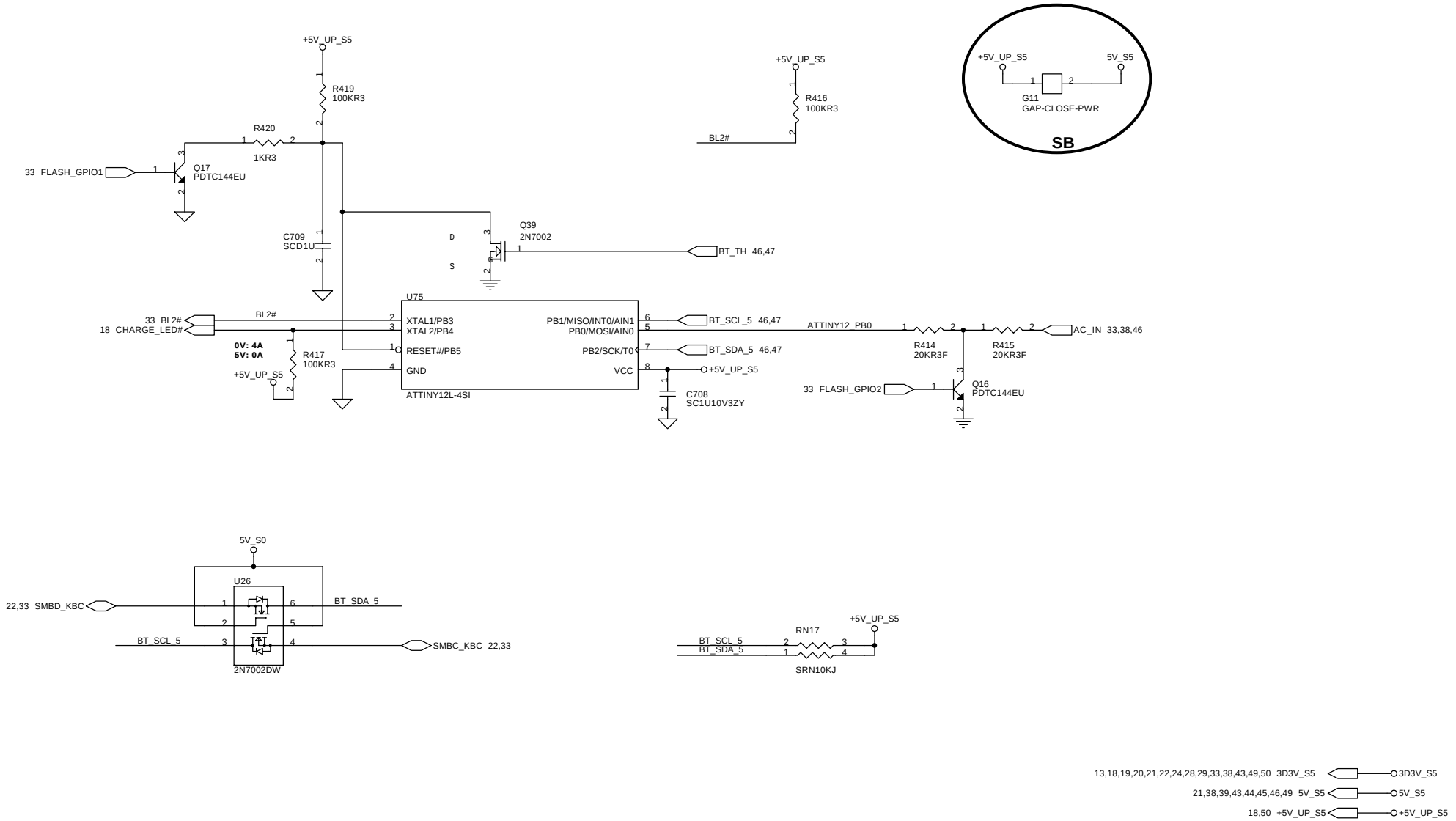

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Micro-P Tiny 12***	
Size A3	Document Number **EGRET**	Rev **SC**
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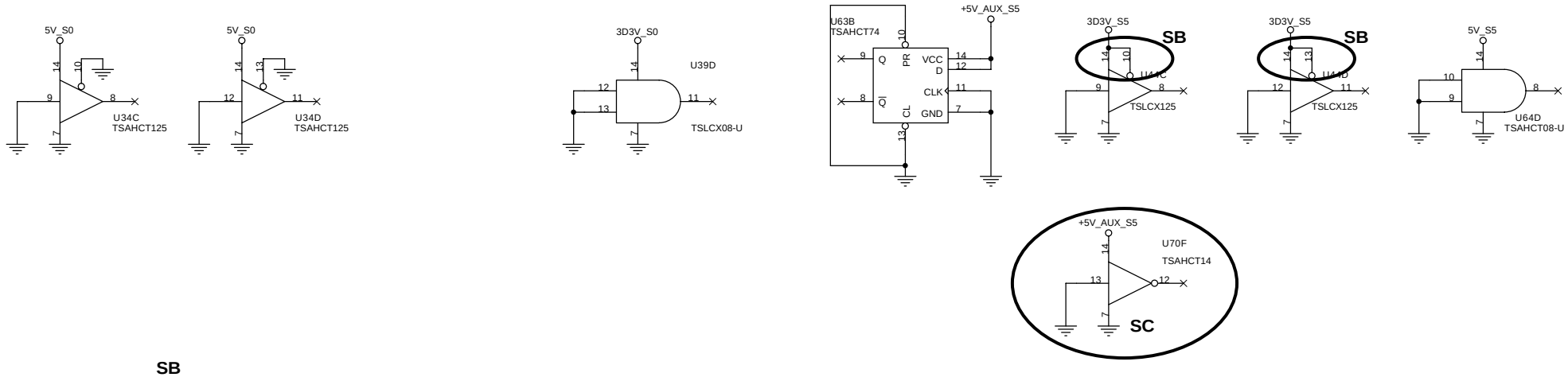
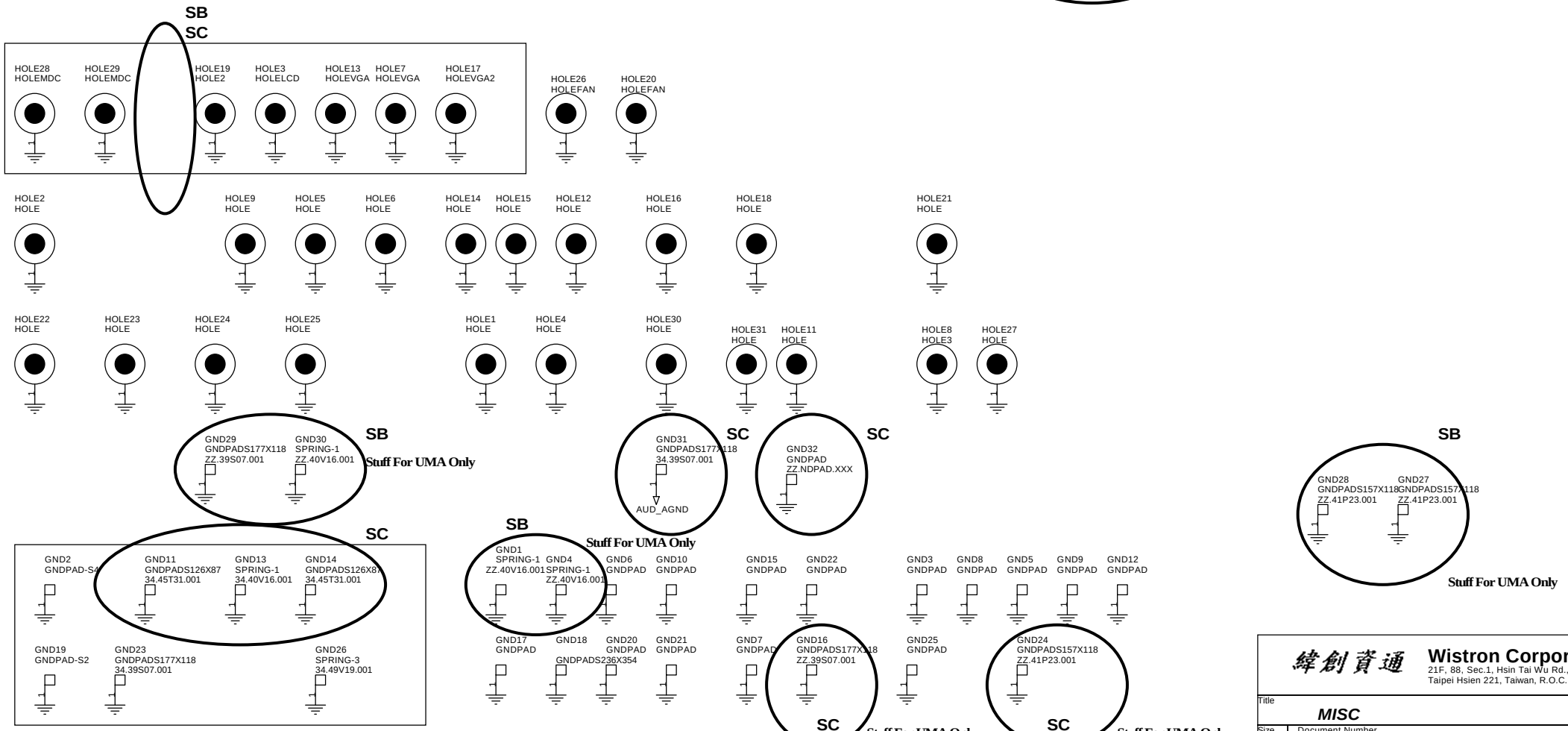
NO USE LOGIC





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Title	***MISC***	
Size A3	Document Number EGRET	Rev **SC**
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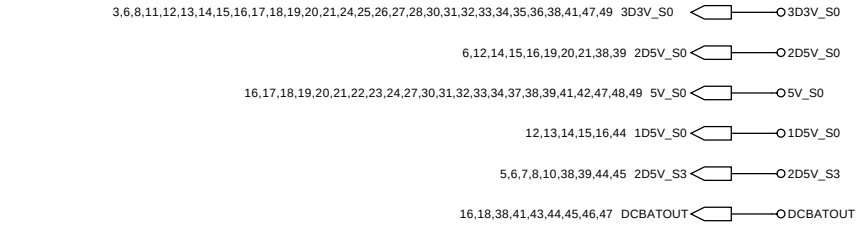
SB

3D3V_S0: 30 pcs
2D5V_S0: 8 pcs
5V_S0: 10 pcs
1D5V_S0: 4 pcs
2D5V_S3: 10 pcs
DCBATOUT: 10 pcs

SB

FOR EMI
DECOUPLING CAPS



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Taipei Hsien 221, Taiwan, R.O.C.

Title: EMI

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